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The Design of Transformer (Dimond Ring) Read-Only Stores

Abstract: The operation of transformer read-only stores is explained and the main methods of construction described. The optimum turns ratio of the transformers is calculated. It is shown how a transformer can produce an output current even though the energised word line is not threaded through it. The value of this ZERO current depends on the information pattern and is found to be greatest with one of two patterns, depending on the type of construction used. For both patterns, expressions for the maximum ZERO and minimum ONE output signals are derived.

The cause of resonances is explained and a method of damping described. The expressions for optimum turns ratio, maximum ZERO and minimum ONE output signals are modified to take account of the damping and a worked example is given. Computed and observed output waveforms are compared for a store containing a non-worst-case pattern and are found to agree well.

Principal symbols

a	turns ratio
a_{opt}	optimum turns ratio
b	number of modules
C	capacitance per element
f_0	fundamental resonant frequency
f_1	lowest frequency of interest
f_2	highest frequency of interest
i_{in}	instantaneous input current
i_{max}	peak value of input current
i_s	instantaneous sense amplifier input current
I_{in}	input current (ac rms value)
I_{p0}	transformer primary current (ac rms value) representing ZERO signal
I_{p1}	transformer primary current (ac rms value) representing ONE signal
I_{s0}	sense amplifier input current (ac rms value) representing ZERO signal
I_{s1}	sense amplifier input current (ac rms value) representing ONE signal
k	coupling factor between primary and secondary of transformer
L_p	inductance of transformer primary
L_s	inductance of transformer secondary
m	number of words in a module
n	number of binary digits in a word
R_d	damping resistance per element
R_s	input resistance of sense amplifier
t	time
t_p	duration of flat portion of input pulse
t_r	rise-time of input pulse
Z	impedance introduced into word line by one transformer and its load
Z_0	characteristic impedance
γ	propagation constant
ω	angular frequency
ω_1	$2\pi f_1$
ω_2	$2\pi f_2$

1. Introduction

Read-only stores have been used for many years in telephone systems and digital computers. Their purpose is to store fixed information such as code translations, subroutines, control microprogrammes, etc. Many different types have been devised, each with advantages and disadvantages, depending on the application. The various types are discussed in an earlier paper.[1]

In several read-only stores the operation depends on the presence or absence of mutual inductance between two

circuits to determine respectively whether a binary ONE or ZERO is stored. One of them, first described by T. L. Dimond in 1951, has become known as the "Dimond ring" or transformer read-only store.[2] Figure 1a shows the operation of a store containing three words, each having four binary digits. There is one conductor, called a *word line* for each word stored, and one transformer core for each digit in the output word. A word line either threads through or bypasses a core, depending on whether the corresponding digit in that word is respectively ONE or ZERO. Thus the information in Word No. 1 is 1011, that in Word No. 2, 0101, and so on.

To read out a word, a current pulse is passed through the corresponding word line. This causes an output current, representing ONE, to appear from the transformers through which the word line is threaded. Ideally it should cause no output current from the remaining transformers but in practice it does so, because of the impedance of the word lines and the capacitance between them. These ZERO currents must be kept small compared with the normal ONE currents.

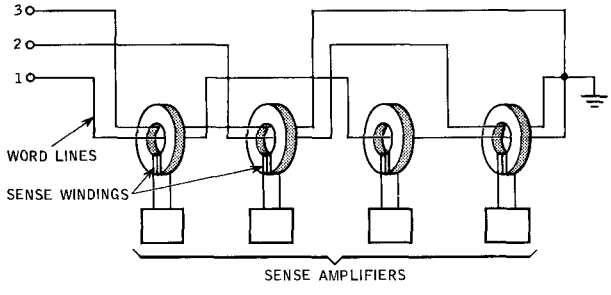
Dimond's original store was used for code translations in the American No. 5 crossbar telephone system, and for subroutines in the Bell Laboratories' Model 6 computer.[3] More recent uses[4,5] include the Atlas ground guidance computer, the stabilization data computer for Polaris submarines, and the model IBM 360/40, where it stores the control microprogramme.

The main attractions of this read-only store compared with others are the simplicity of its construction and the large output signals available. On the other hand it is not as fast as some of the others—the shortest cycle time for a 10^5 bit store is about 0.6 μs—and in some designs it is not easy to alter the stored information.

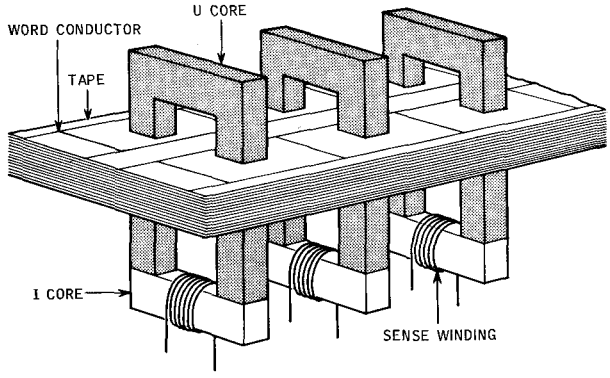
This paper is concerned mainly with electrical aspects of transformer read-only stores and particularly with the calculation of the ZERO currents mentioned above. Methods of construction are described and some details of the store in the model IBM 360/40 are given. The cause of the ZERO current is explained, and its value is shown to be greatest with one of two information patterns, depending on the type of construction used. Equivalent circuits are derived for both these patterns and are analysed by conventional means.

It is found that resonances can occur with "worst-case" patterns and many other regular patterns. An explanation of their cause is given and it is shown how they can be damped out. Finally, the analytical approach used in the paper is verified by comparing computed and observed output waveforms from a particular store.

Figure 1 **Transformer read-only store.** (a) *General configuration;* (b) *Portion of read-only store using printed circuit tapes. In practice the core window is entirely filled but for clarity is shown here partly filled.*



(a)



(b)

2. Construction

Transformer read-only stores are usually made by one of the following methods. In the first method, the cores, usually made of ferrite, are arranged in a row or around the circumference of a circle,[1] and enamel-insulated copper wires are used as the word lines. The wires are usually threaded through the cores by hand, but during the last few years machines for doing it automatically have been developed.

In the second method of construction,[6] the copper wires are replaced by flexible printed circuit tapes as shown in Fig. 1b. Each transformer core consists of a U-shaped and an I-shaped piece, and each tape accommodates two word lines, one associated with each limb of the U core. The tapes are made by bonding copper to a flexible substrate such as Mylar* film, and etching so as to leave two ladder-shaped conductors as shown in Fig. 2. At each core position along the tape, holes are punched in one string of the ladder or the other, depending on whether a ZERO or ONE is to be written in that position. Thus in Fig. 2 the information in the upper word line is ...100110..., and in the lower one ...000111, ... As an alternative to punching holes, the unwanted parts of the ladder can be etched away as part of the printed circuit process.

* Mylar is a trade mark of the DuPont Corporation.

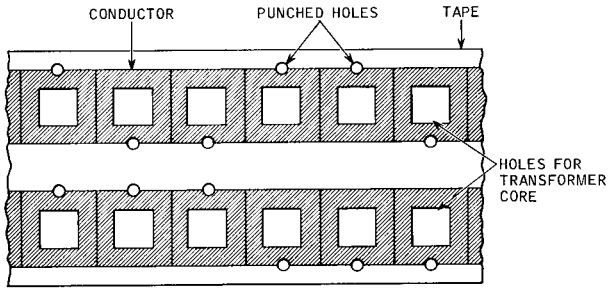
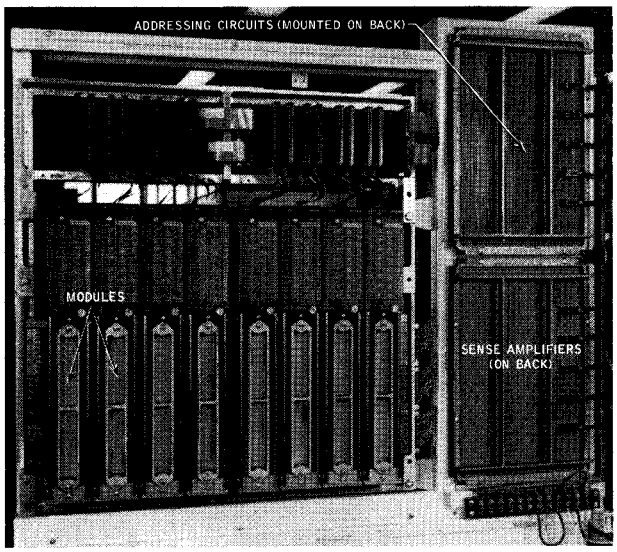


Figure 2 **Word tape.**

Figure 3 **Complete store for IBM System/360 Model 40.** *A second set of eight modules is mounted behind the eight shown.*



There is clearly a limit to the number of tapes that can be accommodated if the limbs of the U core are not to become too long; very long limbs would make the cores fragile and the leakage inductance high. If more tapes are required than can be accommodated on one set of transformers, a modular form of construction is used. Each module consists of a full set of transformers, one for each bit in the output word, but it houses only a proportion of the total number of word tapes. The sense windings of corresponding transformers in each module are connected in parallel.

The stores for the Model IBM 360/40 are of this type. The Model 40 store is shown in Fig. 3. It consists of sixteen modules, each as shown in Figs. 4a and 4b, and the construction of the individual transformers and the method of mounting them are shown in Fig. 5. The following features are worth noting.

1) The row of transformers is folded back on itself so that connections are made only at one end of the tapes.
2) A non-shorting copper sleeve is threaded over each limb of the U cores, as shown in Fig. 6. This reduces leakage inductance.
3) Capacitance between conductors on successive tapes is reduced by staggering them with respect to one another. Three conductor positions are used, as shown in Fig. 7a.
4) In addition to the word tapes there is one tape with a resistive loop (Eureka) around each core hole as shown in Fig. 7b. Its purpose is to damp out resonances, the cause of which is explained in Section 7.

Each module accommodates 128 word tapes, each storing two words. The read-out current is 66 mA and there are 35 turns on each sense winding.

The complete store operates with a cycle time of 625 ns, and has a total access time (including address decoding and delays through the sense amplifier and output latch) of 240 ns.

3. Optimum turns ratio

The calculation of optimum turns ratio will be simplified by ignoring all stray capacitances, and so the only word line that need be considered is the one through which the read-out current is passed. The others are open-circuit and therefore carry no current. For generality, a multimodule store consisting of b modules will be assumed.

The equivalent circuit is shown in Fig. 8. Each transformer has a single-turn primary of inductance L_p and an a-turn secondary of inductance L_s, where $L_s = a^2 L_p$. The coupling factor between them is k. The primary windings are connected in series and driven from a current source i_{in}, and each secondary is loaded by a resistance R_s in parallel with an inductance $L_s/(b-1)$. R_s represents the input resistance of the sense amplifier and $L_s/(b-1)$ the secondary winding inductance of corresponding transformers in the remaining $b-1$ modules.

Assuming a trapezoidal input pulse, i_{in}, as shown in Fig. 9, the waveform of the load current i_s will be calculated. During the rise-time of i_{in},

$$i_{in}(t) = \frac{t}{t_r} i_{max} \tag{3.1}$$

and between t_r and $t_r + t_p$,

$$i_{in}(t) = i_{max}. \tag{3.2}$$

For a single transformer, the load resistance and inductance can be referred to a single turn winding and the transformer itself represented as a T-network of inductances as shown in Fig. 10a. The pi-network of inductances kL_p, $(1-k)L_p$ and $L_p/(b-1)$ are now transformed into the equivalent T-network giving the circuit shown in Fig. 10b.

Analysing this circuit by any of the standard methods,

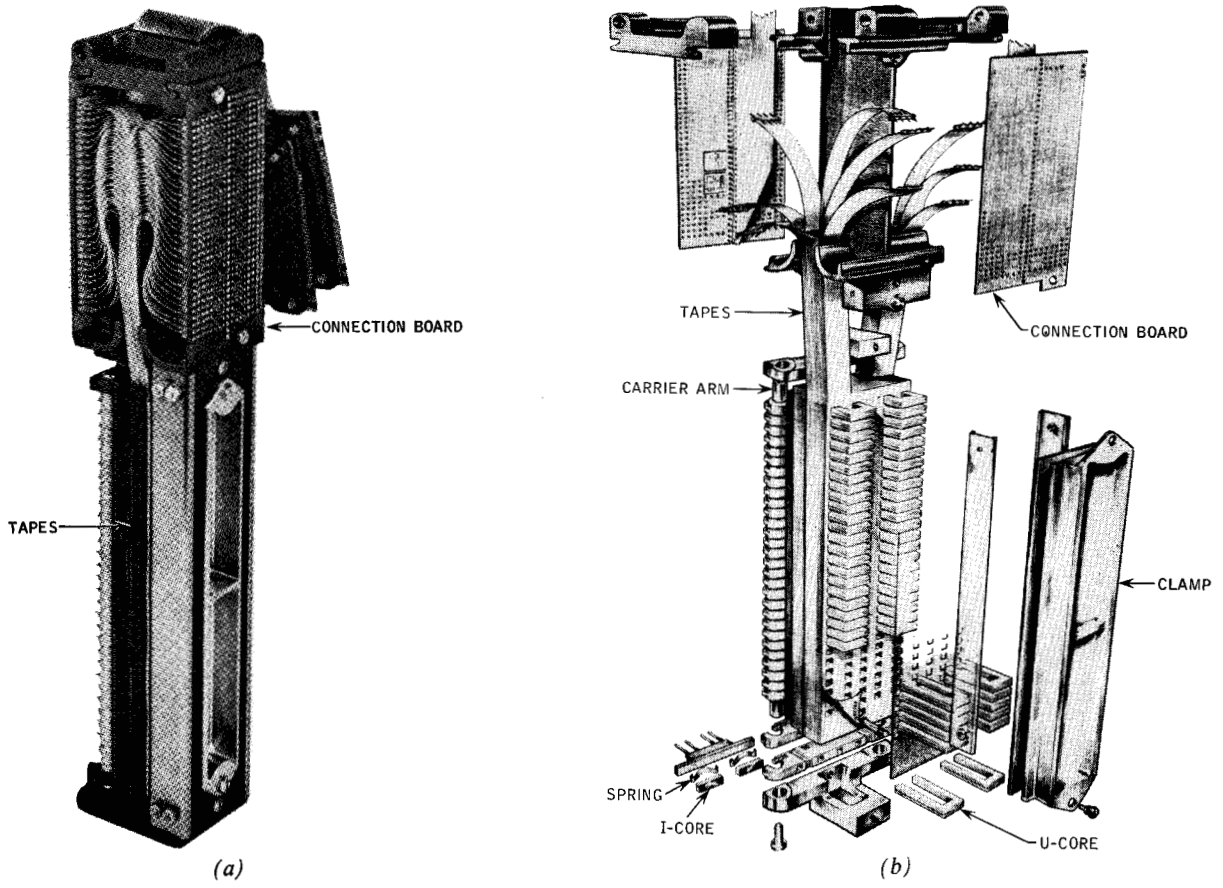


Figure 4 **Module of IBM System/360 Model 40 store.** (a) *Assembled;* (b) *Exploded view. (See text).*

Figure 5 **Pair of transformers (detail).**

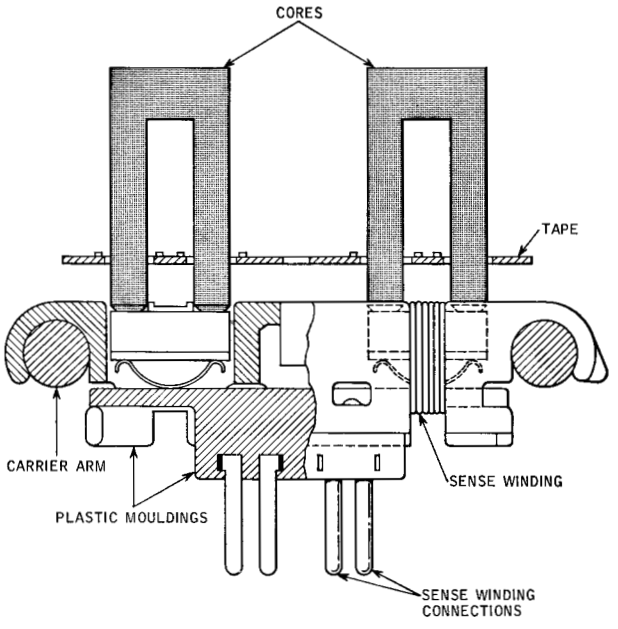
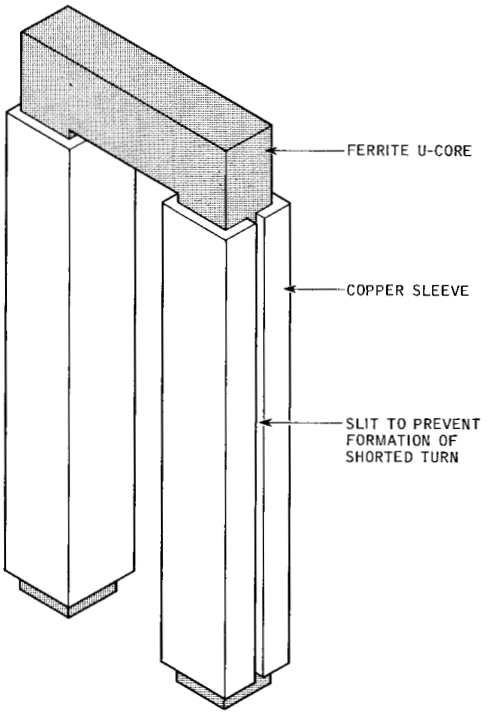


Figure 6 **U-core with copper sleeves.**



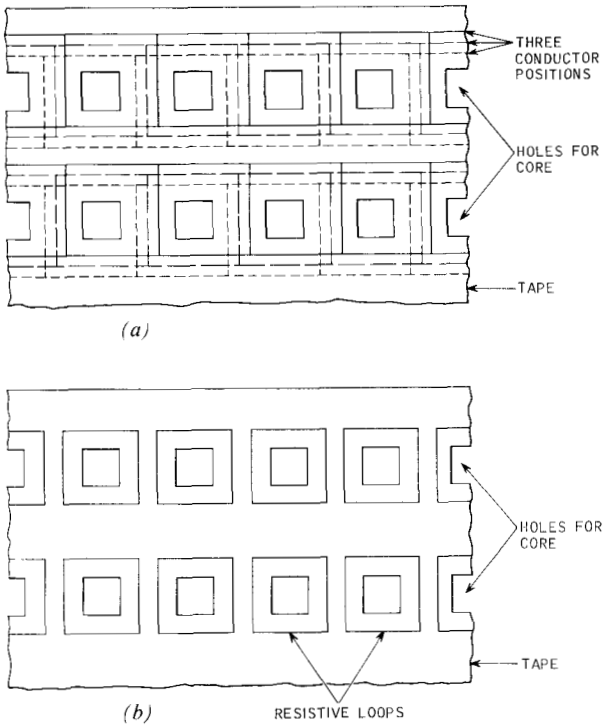


Figure 7 **Details of word tape.** (a) *Portion showing three possible conductor positions. The stagger between successive conductors is 0.026" and the conductor width 0.010".* (b) *Resistive tape.*

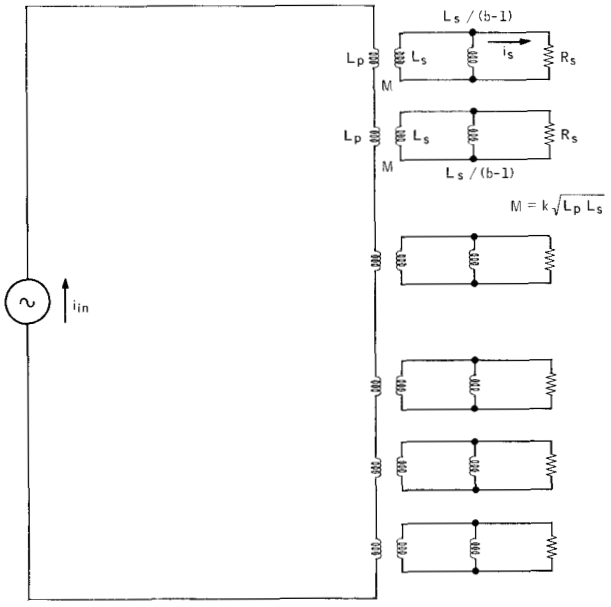
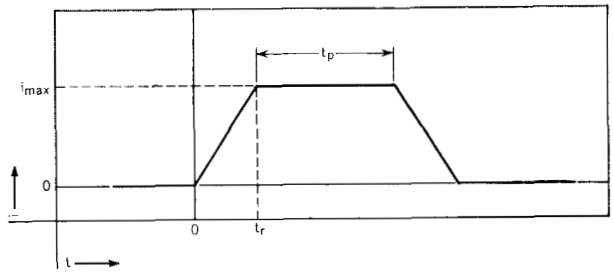


Figure 8 **Simple equivalent circuit of multimodule store**

Figure 9 **Trapezoidal input pulse.**



it can be shown that, when $0 < t < t_r$,

$$i_s(t) = \frac{kaL_p i_{\max}}{bt_r R_s}\left[1 - \exp\left(-\frac{bR_s t}{a^2 L_p}\right)\right]. \tag{3.3}$$

During the interval $t_r < t < (t_r + t_p)$, the $i_s(t)$ decays exponentially according to the equation

$$i_s(t) = i_s(t_r)\exp\left[-\frac{bR_s}{a^2 L_p}(t - t_r)\right]. \tag{3.4}$$

Load current i_s must normally exceed a given threshold value for a certain minimum time in order to operate an output latch circuit. We are therefore particularly interested in its value when $t = t_r + t_p$.

Setting $t = t_r$ in (3.3) and substituting this equation in (3.4),

$$i_s(t_r + t_p) = \frac{kaL_p i_{\max}}{bt_r R_s}\left[1 - \exp\left(-\frac{bR_s t_r}{a^2 L_p}\right)\right]\exp\left(-\frac{bR_s t_p}{a^2 L_p}\right). \tag{3.5}$$

It is shown in Appendix A that there is a value of a for which $i_s(t_r + t_p)$ is a maximum. When $t_p > t_r$, as is usually the case, this value is

$$a_{\text{opt}} \doteqdot \sqrt{\frac{2bR_s(t_r + t_p)}{L_p}}, \tag{3.6}$$

and the maximum value of $i_s(t_r + t_p)$ is

$$[i_s(t_r + t_p)]_{\max} \doteqdot \frac{ki_{\max}}{a_{\text{opt}}}\exp\left[-\frac{t_p}{2(t_r + t_p)}\right]. \tag{3.7}$$

Thus, for $[i_s(t_r + t_p)]_{\max}$ to be high, a_{opt} must be kept low. From (3.6), this means that R_s must be low and L_p high. R_s can usually be kept below 10 ohms by using a grounded-base input stage in the sense amplifier.

4. Conditions for maximum ZERO signal

It was pointed out in Section 1 that an output signal can be obtained from a transformer even though the energised word line is not threaded through it. The cause of this ZERO signal and the factors governing its amplitude will now be discussed.

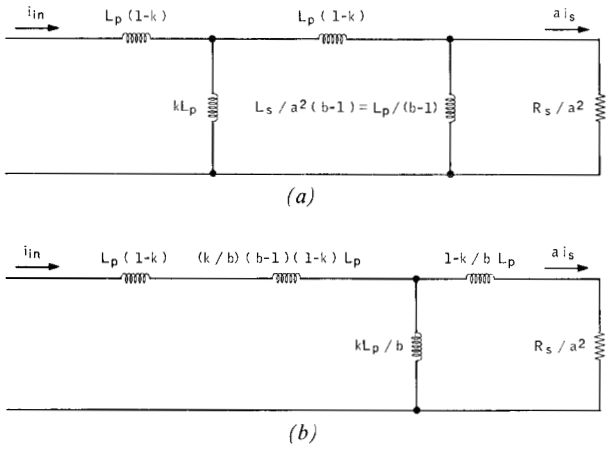


Figure 10 **Equivalent circuit of one transformer and its load.** (a) *Transformer represented by T-network of inductances.* (b) *Pi-network of inductances transformed into T-network.*

First, consider the very simple read-only store shown in Fig. 11. It consists of five transformers T_1 to T_5, and only two word lines p_1 and q_1. p_1 is threaded through T_3 and T_4, and q_1 is threaded only through T_5. The two lines run side by side past T_1 and T_2, which introduces a capacitance C_1 between them.

When a current pulse is applied to p_1 an emf is developed across it owing to the impedance introduced by T_3, T_4 and their load resistors (see Appendix C), and to stray inductance effects. This causes a current to flow through C_1 and along q_1, giving rise to a ZERO signal from T_5.

Now suppose that there are several lines p_2, p_3 ... etc. similar to p_1, i.e., threading T_3 and T_4 only, and q_2, q_3 ... etc. threading T_5 only. When a current pulse is applied to p_1, emf's will be induced in all the p lines as they are all threaded through T_3 and T_4. The total capacitance between the p lines and q lines will be greater than that between the two original lines, causing a larger ZERO signal to be obtained, and the more thoroughly the p and q lines are interleaved, the larger will this signal become.

The magnitude of the ZERO signal is seen to depend on two main factors:

1) the magnitude of the emf induced in the p lines, and
2) the capacitance between the p lines and q lines.

For the capacitance to have the greatest effect it should be confined as far as possible to the high-potential end of the p lines, i.e., the end nearest T_1 in Fig. 11.

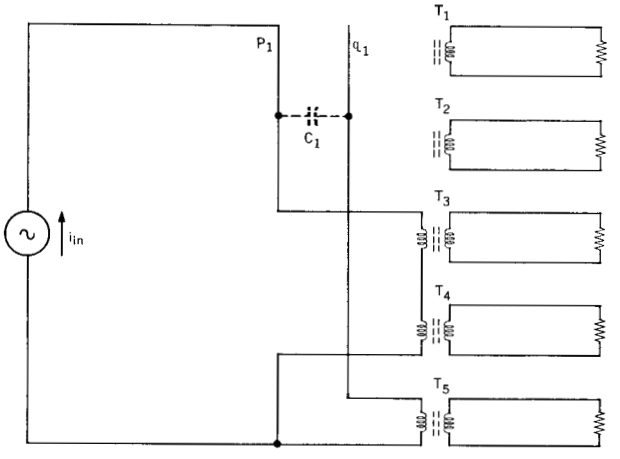
These points will now be considered in relation to the methods of construction described in Section 2. With either method the induced emf in the p lines is highest when they store nothing but ONES. The capacitance between the p and q lines depends on the method of construction. When wires are used as the word lines, or when tapes are used with all the surplus copper etched away, the capacitance between the p and q lines exists mainly where they run close to each other, i.e., where both sets store the same information. It is greatest when they are thoroughly interleaved and when the length of the word lines is greatest. This occurs when they are threaded in and out of the transformers as often as possible, storing the information 1010 ...

Taking the above factors into account we should expect the worst-case pattern for this form of construction to be as shown in Fig. 12. Between transformers T_1 and $T_{n-n'-1}$ all lines store 1010..., and between $T_{n-n'}$ and T_n all p lines store 111...110, and all q lines 000...001. The maximum ZERO signal is obtained from T_n. Its magnitude depends on the relative lengths of the two information patterns, i.e., on the ratio $(n'+1)/n$ (see Fig. 12a), but it is probably greatest when this ratio is about $\frac{1}{2}$. The exact value is a matter for trial.

Now consider the case where printed circuit tapes are used as the word lines and the information is stored by punching holes as shown in Fig. 2. If the punch removes only a small part of the conductor, the total capacitance between the p and q lines no longer depends on the information pattern; all points along the ladder-shaped conductors contribute equally. The ZERO signal is then greatest when the impedance of the p lines is greatest, i.e., where each p line stores 111...110 and each q line 000...001, as shown in Fig. 14 on page 450. The maximum ZERO signal is obtained from T_n, and since the primary current of this transformer has effectively been subtracted from that of T_{n-1}, the latter gives the minimum ONE signal.

Neither of the above patterns would be met in practice but they are worth analysing as limiting cases. The method is to develop equivalent circuits and calculate the ratio

Figure 11 **Simple read-only store.**



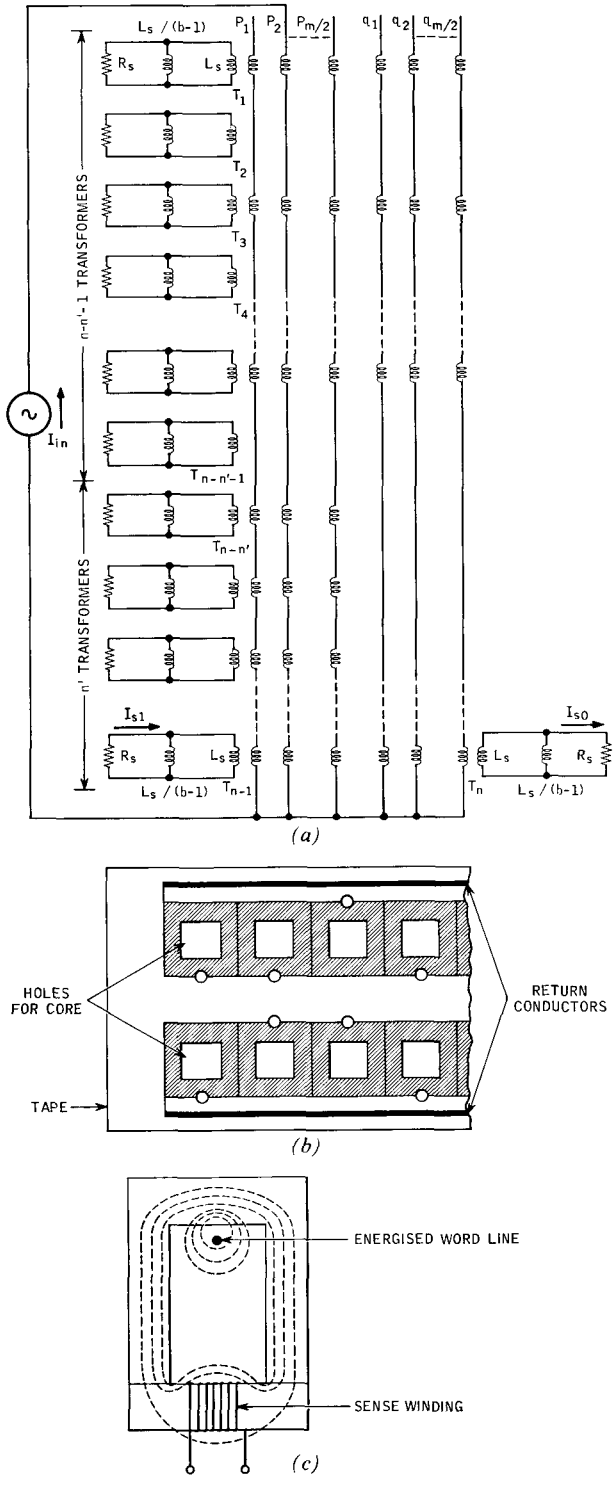


Figure 12 **Store with 1010 . . . 10111 . . . 110/1010 . . . 10000 . . . 001 pattern.** (a) *The p and q lines are interleaved, but are shown separated for clarity. Stray capacitive and inductive coupling between lines is not shown.* (b) *Tape with return conductors for this store pattern.* (c) *Pattern of ϕ_b for this store pattern.*

of the sense amplifier current to input current as a function of frequency, using conventional ac methods. The waveforms of the sense amplifier currents can then be found using Fourier integral techniques.

5. Analysis of store with 1010 . . . 10111 . . . 110/1010 . . . 10000 . . . 001 pattern

We shall consider a store consisting of b modules, one of which contains the 1010 . . .10111 . . .110/1010 . . .10000 . . .001 pattern. In the remaining $b - 1$ modules the capacitances will be ignored and so the information stored in them is immaterial. This arrangement is chosen in preference to the one in which all modules store the above pattern, because it is simpler and in practice gives just as pessimistic a result. (See Section 7).

The arrangement is shown in Fig. 12a. The module under consideration stores m words, each of n bits. All the word lines are threaded through alternate transformers between T_1 and $T_{n-n'-1}$; the p lines then thread through $T_{n-n'}$ to T_{n-1}, and the q lines through T_n only. The p and q lines are thoroughly interleaved and the capacitance between them is assumed to be confined to the region between T_1 and $T_{n-n'-1}$.

A rigorous analysis of this system would be very difficult indeed as one would have to take account of the mutual inductance and mutual capacitance between every possible pair of word lines. However, we can simplify the problem by assuming:

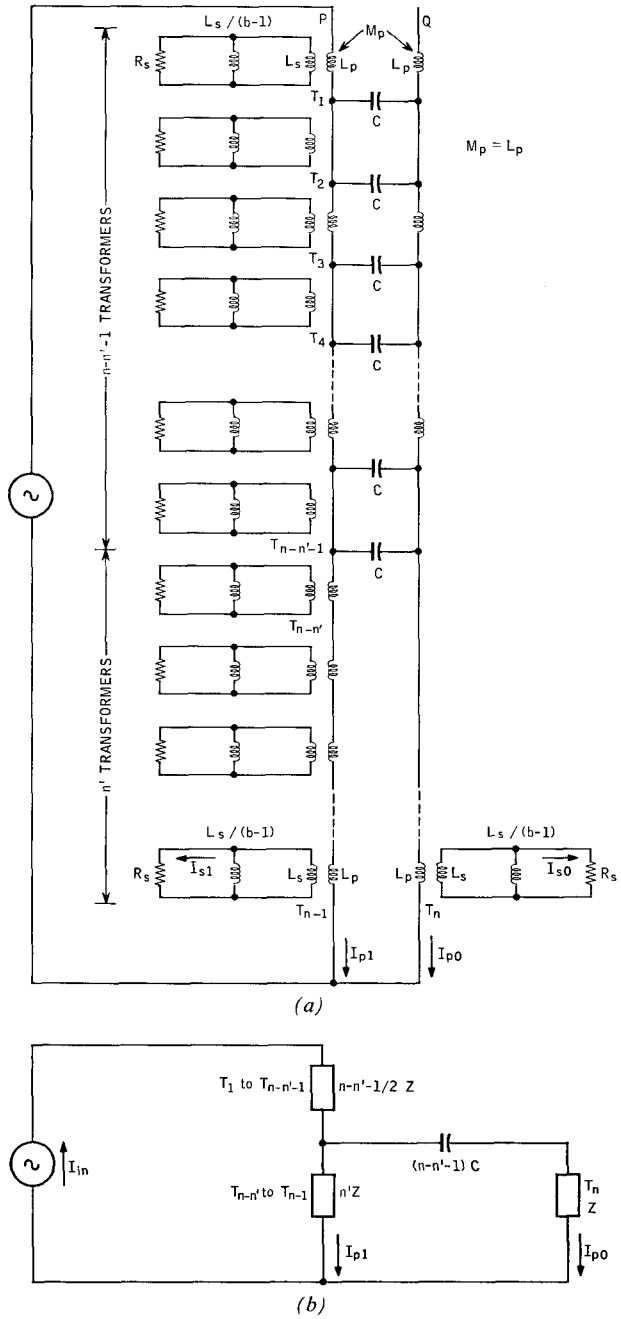
1) that mutual inductance between word lines occurs only when they pass through the same transformer,
2) that the electromagnetic coupling between them is then perfect, and
3) that stray self-inductance of the word lines can be ignored.

In fact the stray inductance of a word line over the length occupied by one transformer is of the same order as the leakage inductance of the transformer. However, it will be seen below that the stray inductances of all word lines threaded through a given transformer act as if they were connected in parallel, and it is really the equivalent parallel inductance that is negligible.

Assumption (1) is valid if each word line with its return circuit encloses very little area, i.e., if the return circuit is taken very close to the word line. When tapes are used as described in Section 2, this can be done by printing each return conductor alongside the corresponding word line as shown in Fig. 12b.

Assumption (2) is valid if the sense winding occupies only a small part of the core circumference, as is usually the case. The magnetic flux in the transformer can be divided into two parts: ϕ_a, the magnetising flux and ϕ_b the leakage flux. The flux ϕ_a passes entirely through the core material and therefore links all the word lines. If the

sense winding is short, ϕ_b remains within the core material except near the energised word line and near the sense winding. Its pattern is shown in Fig. 12c. The portion of ϕ_b near the word line links with few other word lines; it therefore manifests itself mainly as a stray inductance which, from assumption (3) above, we can ignore. On the other hand, the portion of ϕ_b near the sense winding links nearly all the word lines. Thus, apart from a portion of ϕ_b which has no significance, all the flux produced by the energised word line links with every other word line passing through the same transformer.



All the p lines in Fig. 12a may therefore be assumed to be perfectly coupled, and so also may all the q lines. This allows us to represent all the p lines by a single line P and the q lines by a single line Q, as shown in Fig. 13a. The capacitance between P and Q will be that between the parallel combination of all the p lines and the parallel combination of all the q lines over the length where they run close together, i.e., from transformer T_1 to $T_{n-n'-1}$. If the capacitance between them over the length occupied by one transformer is C, the total capacitance will be $(n - n' - 1)C$.

Between T_1 and $T_{n-n'-1}$ lines P and Q are assumed to be perfectly coupled, and so the emf induced in any element of P is the same as that induced in the corresponding element of Q. The potential difference between these elements is therefore constant, regardless of their position along this part of the system, and so the total capacitive current between P and Q is the same as if the capacitance between them were concentrated at any one point. Let us assume it to be concentrated between $T_{n-n'-1}$ and $T_{n-n'}$. Then, representing the impedance introduced into P or Q by each transformer and its load as Z, whose value is calculated in Appendix C (Eq. C.1), the complete equivalent circuit is as shown in Fig. 13b.

The required current transfer ratios are calculated in Appendix D. They are:

$$\frac{I_{s0}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \dfrac{bR_s}{j\omega a^2 L_p}} \cdot \frac{j\omega(n - n' - 1)n'CZ}{1 + j\omega(n - n' - 1)(n' + 1)CZ} \tag{5.1}$$

and

$$\frac{I_{s1}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \dfrac{bR_s}{j\omega a^2 L_p}} - \frac{I_{s0}}{I_{in}}, \tag{5.2}$$

Z being given by (C.1).

6. Analysis of store with 111 . . . 110/000 . . . 001 pattern

As in Section 5, we consider a store consisting of b modules, one of which stores the relevant pattern, 111 . . .10/000 . . .01 in this case, and we ignore capacitances in the remaining $b - 1$ modules. The store is shown in Fig. 14. Following the argument used in Section 5, all the p lines are represented by a single line P, all the q lines by a single line Q,

Figure 13 **Simplified case of Fig. 12a.** (a) *Equivalent circuit, in which the capacitance between P and Q over the region T_1 to $T_{n-n'-1}$ is uniformly distributed. Its total value is $(n - n' - 1)C$.* (b) *Complete equivalent circuit.*

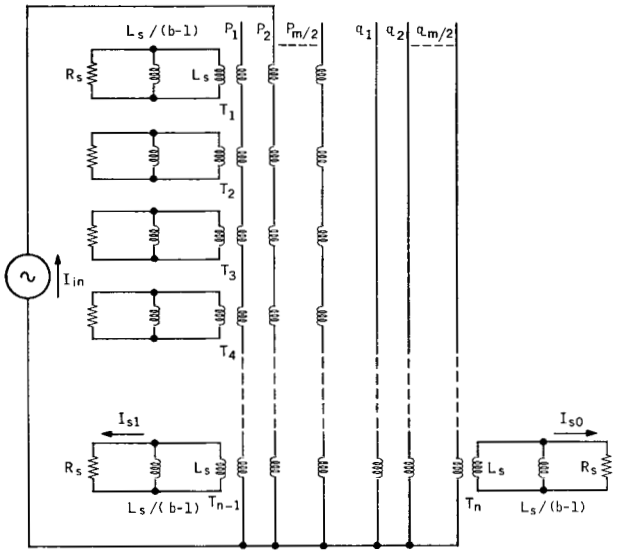
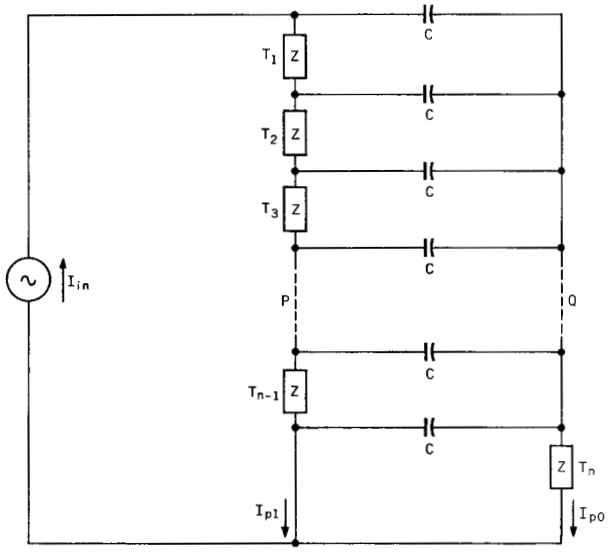
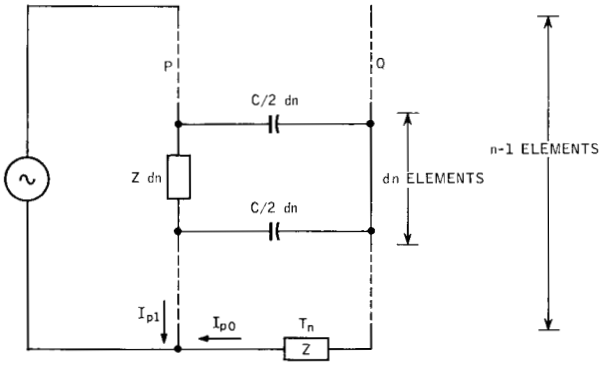


Figure 14 **Store with 111 . . . 110/000 . . . 001 pattern.**

Figure 15 **Equivalent circuits.**



(a)



(b)

and each transformer and its load by an impedance Z, whose value is given by (C.1) (Appendix C). This gives the circuit shown in Fig. 15a. As explained in Section 4, the maximum ZERO signal will be obtained from T_n and the minimum ONE from T_{n-1}, and so we are interested in the currents in P and Q, I_{p1} and I_{p0}, at the end of the system where these lines are commoned.

Although the capacitance between P and Q is shown lumped, it is in reality almost uniformly distributed. Assuming it to be perfectly uniform, the system between T_1 and T_{n-1} can be regarded as a transmission line with series impedance Z per element, shunt capacitance C per element, and length $(n-1)$ elements, an element being defined as the length of the system occupied by one transformer. The final equivalent circuit is therefore as shown in Fig. 15b.

The required current transfer ratios are calculated in Appendix E. They are:

$$\frac{I_{s0}}{I_{\text{in}}} = \frac{k}{a}\cdot\frac{1}{1+\dfrac{bR_s}{j\omega a^2 L_p}} \cdot\frac{\cosh\gamma(n-1)-1}{\cosh\gamma(n-1)+\dfrac{Z}{Z_0}\sinh\gamma(n-1)} \tag{6.1}$$

and

$$\frac{I_{s1}}{I_{\text{in}}} = \frac{k}{a}\cdot\frac{1}{1+\dfrac{bR_s}{j\omega a^2 L_p}} - \frac{I_{s0}}{I_{\text{in}}}, \tag{6.2}$$

where Z is given by (C.1) and where

$$\gamma = \sqrt{Z.j\omega C}, \text{ and} \tag{6.3}$$

$$Z_0 = \sqrt{\frac{Z}{j\omega C}}. \tag{6.4}$$

7. Array resonances

7.1 *Causes and cure*

It is shown in Appendix C that in a multimodule store each transformer can behave like a pure inductance of value $L_p(1-k^2)$, i.e., as if its sense winding were short-circuited. This is true throughout the frequency range when there are many modules [$b \gg k^2/(1-k^2)$] and in the upper part of the frequency range when the number of modules is not so great. The result of this is to give the circuits analysed in Sections 5 and 6 one or more resonant frequencies.

If the input pulse I_{in} contains significant components at these frequencies the ONE and ZERO output waveforms will be as shown in Fig. 16. The ratio between them will be too low, and the persistence of the oscillation will limit the speed of the store.

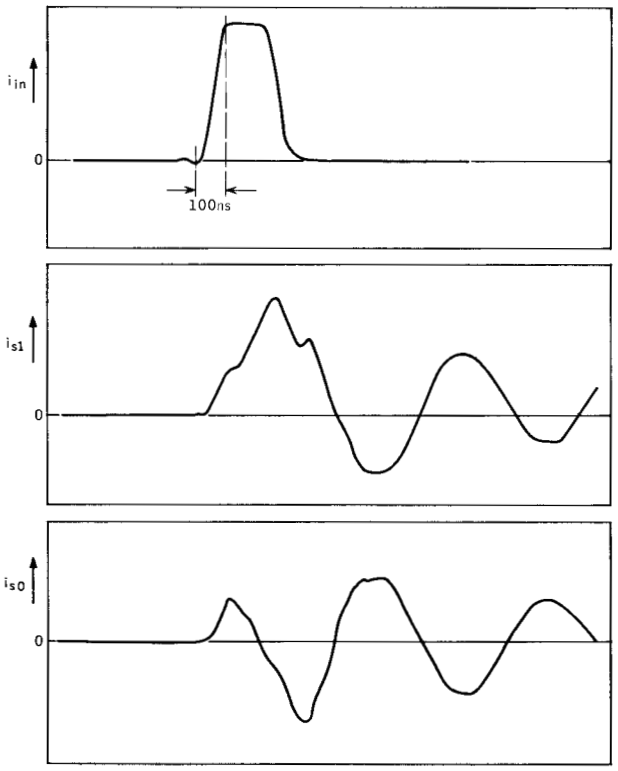


Figure 16 **Output waveforms showing effect of resonance.** *These were obtained from the module used for the experiment in Section 9, with resistance tape removed. The fundamental resonant frequency is about 3 Mc/s.*

The resonances may be damped out as follows. Each transformer, as mentioned above, behaves as though its sense winding were short circuited; therefore the only significant flux is the leakage flux ϕ_b, whose pattern is shown in Fig. 12c. Following the argument given in Section 5, the only part of the leakage flux that we need consider is the part that remains within the core material except in the immediate neighbourhood of the sense winding. To damp out the resonance this flux must be linked by a resistive winding.

When printed circuit tapes are used for the word lines, the resistive windings may be made in a similar way to the word lines themselves. A sheet of Eureka, instead of copper, is bonded to the substrate material and etched so as to leave a loop round each hole through which the transformer cores pass. This resistive tape, shown in Fig. 7b, can be placed anywhere in the stack of word line tapes, except close to the sense windings; if the sense winding is at the bottom of the stack it is usually convenient to place the resistive tape at the top. Every core is linked by two resistive loops, and if each loop has a resistance r, the effective damping resistance is $R_d = r/2$. Assuming that the loops link the entire leakage flux, R_d appears in parallel with the inductance $L_p(1 - k^2)$ which represents the transformer and its load.

We now calculate the values of R_d to give critical damping for the information patterns discussed in Sections 5 and 6. If each impedance Z in Fig. 13b is replaced by an inductance $L_p(1 - k^2)$ in parallel with a resistance R_d, the result is a parallel resonant circuit as shown in Fig. 17a. This is critically damped when

$$R_d = \frac{1}{2(n' + 1)} \sqrt{\frac{(n' + 1)(1 - k^2 L_p)}{(n - n' - 1)C}}. \tag{7.1}$$

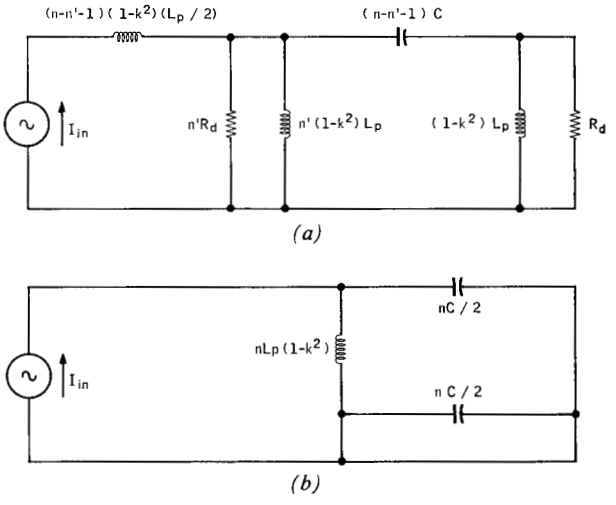
We turn now to the information pattern considered in Section 6. Replacing each impedance Z in Fig. 15 by an inductance $L_p(1 - k^2)$, and remembering that the capacitance between P and Q is uniformly distributed, the system reduces to a lossless transmission line, open-circuit at one end and short-circuit at the other. The fact that the impedance representing T_n is in line Q instead of line P is of no consequence here. This system resonates at a fundamental frequency

$$f_0 = \frac{1}{4n\sqrt{(1 - k^2)L_p C}} \tag{7.2}$$

and its odd harmonics. Of these, only the fundamental frequency is important in practice since if I_{in} contained significant components at the harmonic frequencies the ZERO signal would be too great.

At f_0 the line can be represented fairly accurately by a pi-network as shown in Fig. 17b. The capacitance at the short-circuit end can have no effect, and so the circuit reduces to a simple resonant circuit having an inductance $n(1 - k^2)L_p$ in parallel with a capacitance $nC/2$. The

Figure 17 **Equivalent circuits.**



damping appears as a resistance nR_d across this circuit, and so, for critical damping,

$$R_d = \frac{1}{n}\sqrt{\frac{L_p(1 - k^2)}{2C}}. \tag{7.3}$$

It is unlikely in practice that critical damping would ever be required, even when the stored information approaches the worst-case patterns. A value of R_d twice that given by the relevant equation would probably be satisfactory.

Lastly, we consider resonances in single-module stores. It is shown in Appendix C that when the turns ratio a has its optimum value as given by (3.6) and when $(1 - k^2) = 0.1$, the phase angle of Z does not rise above 65° in the frequency range of interest. Therefore, although a single-module store may be reduced to a resonant circuit by the same arguments as used above, the Q will not exceed tan 65°, i.e., 2.15. This should be quite acceptable.

• 7.2 *Current transfer ratios in damped arrays*

In this section, the current transfer ratio calculations will be revised to take account of damping resistors. As in Sections 5 and 6, we consider a store consisting of b modules, one of which stores the relevant pattern. We ignore capacitances in the remaining modules but assume that all have damping resistors. The equivalent circuit of a transformer in the module and its load is therefore as shown in Fig. 18.

Some of the assumptions made in deriving this model may appear inconsistent with one another. It could be argued, for example, that there is no point in putting damping resistors in $b - 1$ modules unless their stored information tends to cause resonances, and if it does, their internal capacitances should be taken into account. A calculation taking them into account has in fact been made, but it is tedious, and for a given set of parameters it gave a slightly smaller peak ZERO signal than the model now proposed. This happens because in the more complex model the sense amplifier input resistance adds more significantly to the damping. Thus, the proposed model is easier to analyse but gives a slightly pessimistic result.

Referring to Fig. 18a, T_1 is a transformer in the module under consideration and T_2 represents the parallel combination of corresponding transformers in the remaining $b - 1$ modules. We wish to find expressions for the input impedance Z and for the ratio between the sense amplifier current, I_s and the primary current I_p, of T_1. R_s is referred to single-turn windings on T_1 and T_2, and each of these transformers is represented by a pi-network of inductances, as shown in Fig. 18b. The input impedance of this circuit is found to be

$$Z = \frac{1 + Y_cZ_b + \dfrac{b - 1}{1 + 1/Y_aZ_b}}{bY_a + Y_c(1 + Y_aZ_b)} \tag{7.4}$$

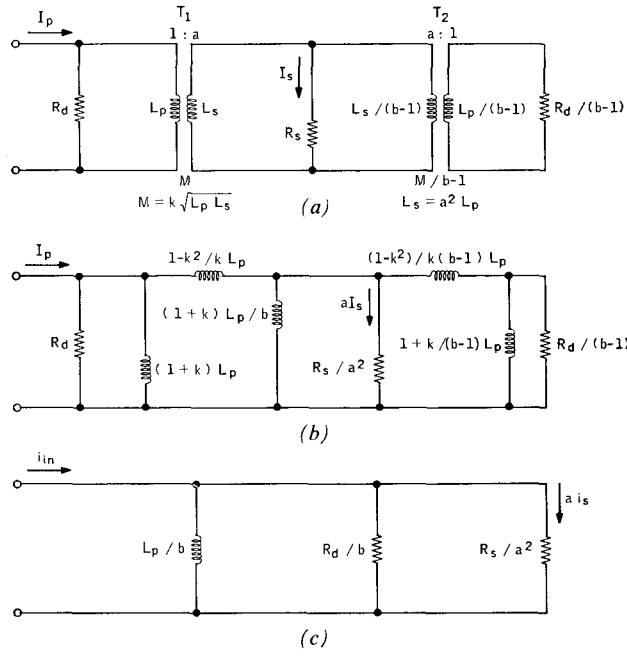


Figure 18 **Transformer and load with damping.** (a) *Equivalent circuit.* (b) *Circuit with transformers represented by pi-network of inductances.* (c) *Simplified equivalent circuit.*

and the ratio of I_s to I_p,

$$\frac{I_s}{I_p} = \frac{a}{R_s[bY_a + Y_c(1 + Y_aZ_b)]}, \tag{7.5}$$

where

$$Y_a = \frac{1}{R_d} + \frac{1}{j\omega(1 + k)L_p} \tag{7.6}$$

$$Z_b = j\omega\frac{1 - k^2}{k}L_p \tag{7.7}$$

and

$$Y_c = \frac{a^2}{R_s} + \frac{b}{j\omega(1 + k)L_p}. \tag{7.8}$$

The transfer ratios I_{p0}/I_{in} and I_{p1}/I_{in} in the worst-case modules are still as given by (D.1), (D.2), (E.12) and (E.13) but the value of Z to be used in them and in (E.4) and (E.5) is now given by (7.4). The corresponding expressions for I_{s0}/I_{in} and I_{s1}/I_{in} are

$$\frac{I_{s0}}{I_{in}} = \frac{I_{p0}}{I_{in}}.\frac{I_s}{I_p}, \text{ and} \tag{7.9}$$

$$\frac{I_{s1}}{I_{in}} = \frac{I_{p1}}{I_{in}}.\frac{I_s}{I_p} \tag{7.10}$$

where I_s/I_p is given by (7.5).

• 7.3 *Optimum turns ratio in damped arrays*

It is important to note that when damping resistors are used the optimum turns ratio is no longer as given by (3.6). An exact calculation of the new value would be very tedious, but it can be simplified by assuming that the coupling between word lines and sense windings is perfect, i.e., $k = 1$. The equivalent circuit of a transformer and its load in Figs. 18a and 18b then simplifies to that shown in Fig. 18c.

If we apply a trapezoidal input pulse as shown in Fig. 9 to this circuit and follow the same method of calculation as in Section 3 and Appendix A, the optimum turns ratio is found to be

$$a_{\text{opt}} = \sqrt{bR_s\left[\frac{t_r + t_p}{L_p} + \sqrt{\left(\frac{t_r + t_p}{L_p}\right)^2 + \left(\frac{1}{R_d}\right)^2}\right]} \tag{7.11}$$

and the maximum value of i_s at the end of the input pulse,

$$[i_s(t_r + t_p)]_{\max} = \frac{i_{\max}}{a_{\text{opt}} + \dfrac{bR_s}{a_{\text{opt}}R_d}} \cdot \exp\left[\frac{-t_p}{t_r + t_p + \dfrac{L_p}{R_d} + \sqrt{(t_r + t_p)^2 + \left(\dfrac{L_p}{R_d}\right)^2}}\right]. \tag{7.12}$$

8. Example

As an example, the calculations in Sections 6 and 7 are now applied to a store with the following characteristics:

Turns ratio	$a = 30$
No. of modules	$b = 16$
No. of bits per word	$n = 60$
Transformer coupling factor	$k = 0.94$
Transformer primary inductance	$L_p = 163\ \mu\text{H}$
Capacitance per element	$C = 89\ pF$
Damping resistance per element	$R_d = 0.33\Omega$
Sense amplifier input resistance	$R_s = 10\Omega$

The input pulse I_{in}, is assumed to be trapezoidal as shown in Fig. 9, with $i_{\max} = 66$ mA and $t_r + t_p = 200$ ns. The calculation is made with $t_r = 40$ and 120 ns.

Input current i_{in} is applied to a module in which each p line stores 111...110, and each q line 000...001. Capacitances in the remaining $(b - 1)$ modules are ignored but each is assumed to have damping resistances, as in Section 7. The output waveforms are shown in Fig. 19.

The ONE waveform is very similar in the two cases; increasing t_r from 40 to 120 ns hardly affects its amplitude but reduces the width somewhat. The effect on the ZERO waveform is far more marked however, and the amplitude of the initial positive pulse is reduced by a factor of nearly 2.

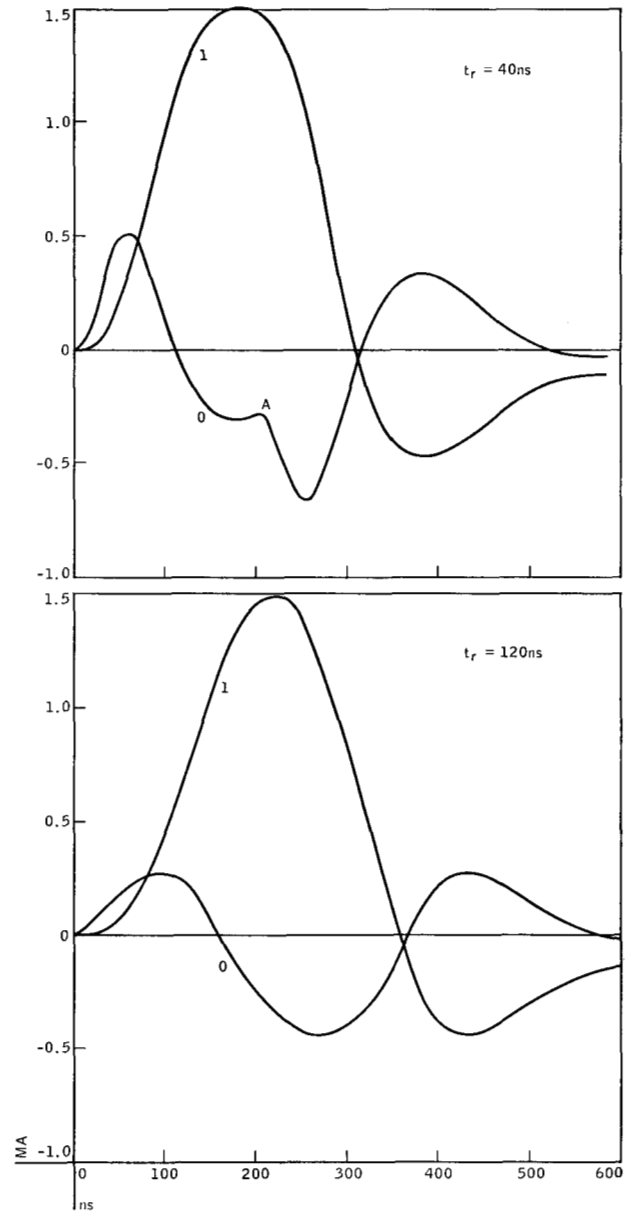


Figure 19 **Output waveforms in the example.** *(See text)*

Examination of the ZERO waveform at $t_r = 40$ ns shows it to consist of two parts, an initial positive pulse followed by a negative pulse caused by the leading edge of the input waveform, and a negative pulse followed by a positive pulse caused by the trailing edge. In the example given, the negative pulse caused by the trailing edge commences just after the negative pulse caused by the leading edge (point A in Fig. 19). This results in a total negative excursion 0.44 times the peak ONE amplitude.

One may be tempted to argue that this is unimportant because the two pulses have opposite polarities, but this

argument would not be justified. Referring to the original circuit of the worst-case pattern in Fig. 14, suppose that the energised word line p_2 was not threaded through T_{n-1}, but that otherwise the circuit was unchanged. T_{n-1} would no longer give a ONE output signal, but otherwise the currents in the circuit would be little changed. This means that the total primary current of T_{n-1} would be equal in magnitude to that of T_n (apart from a small capacitive current), but opposite in direction. T_{n-1} would therefore give a ZERO output signal of almost exactly the same waveform as T_n gives in the above example, but its polarity would be reversed. The peak of the waveform occurring shortly after A would then be of the same polarity as the ONE waveform.

9. Comparison between computed and observed output waveforms

In this section we compare computed and observed output waveforms from a particular module. Ideally we would have chosen to make this experiment on a module storing a worst-case pattern and constructed exactly according to the assumptions in Section 5 or 6; this would have given the best check on the accuracy of the analysis. However, at the time the work was being done no module having the assumed characteristics had been made, and we were obliged to use what was available. The module used had certain constructional differences and did not contain a worst-case pattern. However we were able to analyse it by the same method as before, and so the experiment gives a good check on the validity of this approach.

We used an earlier version of the IBM 360/40 module described in Section 2. It was identical with the later version except that the row of transformers was not folded back on itself. Each p line stored 1010...10 and each q line 0101...01, and the lines were stacked alternately to give the greatest capacitive effect.

Apart from the information pattern, the module differed from those assumed in Sections 5 and 6 in the following respects:

a) The word lines and their return circuits were not run close together. Instead, all word lines used a common return path spaced several inches away. This meant that, contrary to the assumptions in Sections 5 and 6, stray mutual inductance between the word lines could not be ignored.

b) There was stray magnetic coupling between the sense windings of adjacent transformers, owing to their proximity and to the windings enclosing a much greater area than the cross-section of the core (see Fig. 5).

Although stray mutual inductance between the word lines could no longer be ignored, we still assumed, for simplicity, that there was perfect coupling between all the p lines and between all the q lines. They could therefore still be represented by two lines P and Q, the stray mutual inductance between the p lines appearing as a distributed inductance $\frac{1}{2}L_1$ per element in P, that between the q lines as a distributed inductance $\frac{1}{2}L_1$ per element in Q, and that between the p and q lines as a distributed mutual inductance $\frac{1}{2}M_1$ per element between P and Q. An element is defined here as half the length of the system containing a transformer in each of lines P and Q. This makes the total number of elements, n, equal to the number of digits in a word, as in Section 6.

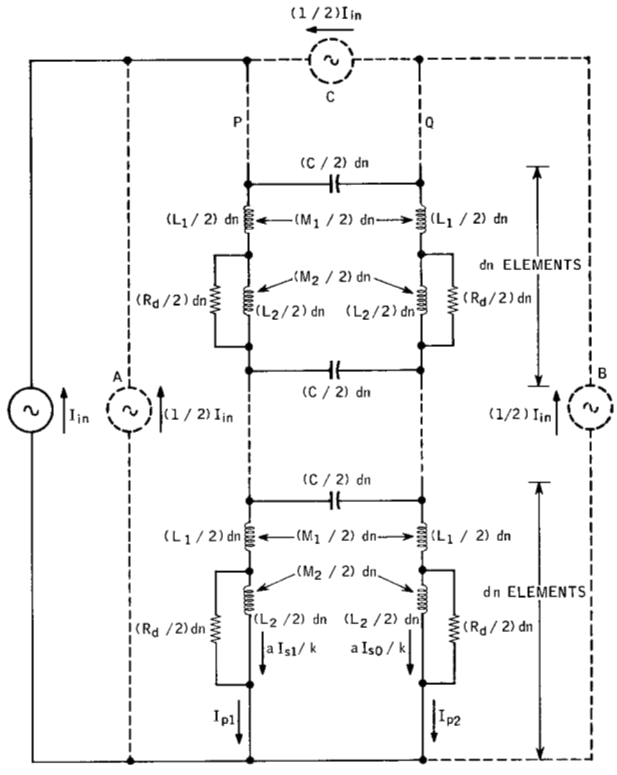
All the sense windings were short-circuited to simulate the effect of a multimodule array (see Appendix C), and damping resistors were fitted. Each transformer could therefore be represented by its leakage inductance L_2, given by

$$L_2 = L_p(1 - k^2) \tag{9.1}$$

in parallel with the damping resistance R_d. The stray coupling between sense windings was allowed for by introducing a mutual inductance between the L_2 elements.

Regarding all the above elements as uniformly distributed, the equivalent circuit of the store is as shown in Fig. 20. It was analysed by replacing the single generator I_{in} by the three shown dotted, A, B and C, each of strength

Figure 20 **Equivalent circuit of module storing 1010 . . . 10/0101 . . . 01 pattern.**



$\frac{1}{2}I_{in}$. First we calculated the output currents produced by A and B acting simultaneously, then by C alone, and we obtained the total output currents by applying the Superposition Theorem. The maximum ZERO current I_{s0} and the minimum ONE current I_{s1} are obtained from transformers T_n and T_{n-1} at the end of the system where P and Q are commoned. They are given by

$$\frac{I_{s0}}{I_{in}} = \frac{kR_d}{2a}\left[\frac{1}{R_d + j\omega(L_2 + M_2)} - \frac{\operatorname{sech}\gamma n}{R_d + j\omega(L_2 - M_2)}\right] \tag{9.2}$$

and

$$\frac{I_{s1}}{I_{in}} = \frac{kR_d}{2a}\left[\frac{1}{R_d + j\omega(L_2 + M_2)} + \frac{\operatorname{sech}\gamma n}{R_d + j\omega(L_2 - M_2)}\right] \tag{9.3}$$

where

$$\gamma = j\omega\sqrt{C\left[L_1 - M_1 + \frac{R_d(L_2 - M_2)}{R_d + j\omega(L_2 - M_2)}\right]}. \tag{9.4}$$

The module had the following parameters:

a = 30
n = 56 elements
k = 0.94 at 2 Mc/s (in the computation k was assumed constant at this figure)
L_1 = 11.3 nH/element
M_1 = 10 nH/element
L_2 = 19.1 nH/element
M_2 = −4.8 nH/element
C = 89 pF/element
R_d = 0.33Ω/element

The waveform of the input current was as shown in Fig. 21a; for the purpose of the computation it was assumed trapezoidal as in Fig. 9, with t_r = 50 ns, t_p = 300 ns, and i_{max} = 46 mA.

The computed and observed output waveforms are shown in Fig. 21b and 21c, and bearing in mind the approximations used in deriving the equivalent circuit, and the lack of refinement in measuring the array parameters, the agreement between them is very good.

An interesting feature of the observed waveforms is a small 6 Mc/s oscillation whose phase is the same for both ONE and ZERO output waveforms. This is a different effect from the one discussed in Section 7 and is probably caused by the series inductance of P and Q resonating with the capacitance between the word lines and sense windings, which are grounded.

10. Conclusions

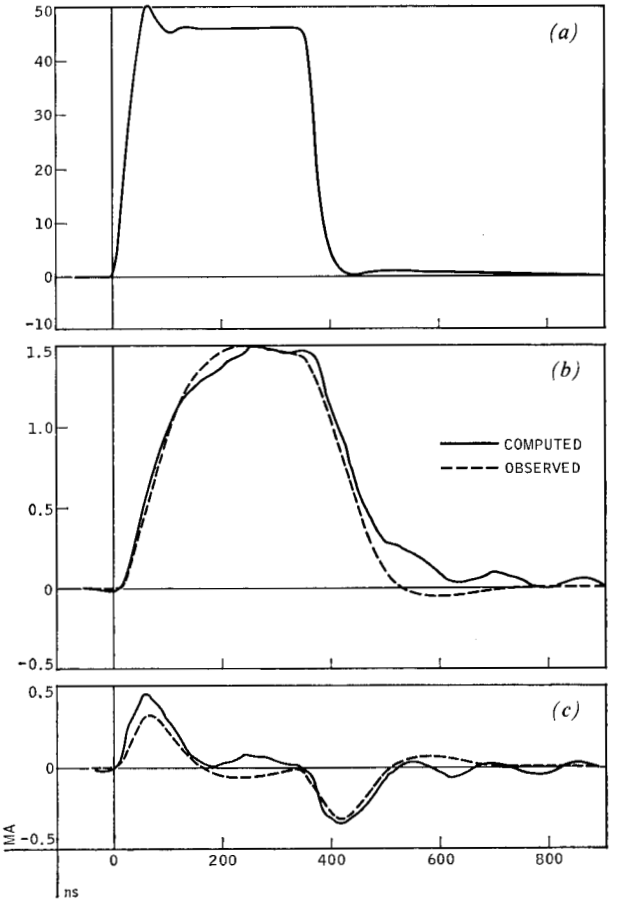
The main purpose of this paper has been to analyse transformer read-only stores under conditions of maximum ZERO signal. Two information patterns have been considered, one giving maximum ZERO signal when ordinary wires are used as the word lines and the other when punched printed-circuit tapes are used.

Equivalent circuits have been derived, and we have shown that they can be simplified to a point where they are easily analysed. Both worst-case information patterns give rise to resonances (as do many other regular patterns) and a method of damping them has been described.

The calculations of maximum ZERO and minimum ONE signals have been supported by comparison with experiment. The comparison was made on a non-worst-case pattern, but the simplifying assumptions and method of analysis were the same as for worst-case patterns. The comparison can therefore be regarded as giving good confirmation of the worst-case results.

The transformer read-only store is attractive in several ways. It is simple and inexpensive to build and gives good output signals without requiring high word-line currents. A microprogramme store of over 10^5 bits capacity has been found to give reliable operation at a cycle time of

Figure 21 **Waveforms:** (a) *Input current.* (b) ONE *output current.* (c) ZERO *output current.*



0.6 μs. Where the highest speeds are not required, or the greatest ease in changing the stored information, the transformer read-only store has much to recommend it.

Acknowledgments

The authors are happy to acknowledge the help they received in discussions with members of the design team concerned with the stores for the IBM System/360, Model 40. They are particularly grateful to J. G. Axford, C. G. J. Dailey and A. Proudman, who were responsible for the electrical design, W. A. Warwick who was responsible for mechanical design, B. A. M. Willcox who wrote programmes for the analysis of the equivalent circuits, and C. E. Owen who acted as consultant to the project.

Appendix A. Optimum turns ratio, and maximum load current at $t = t_r + t_p$

The model used in this calculation is as described in Section 3. To obtain the optimum turns ratio a_{opt}, Eq. (3.5) is differentiated with respect to a, and the differential equated to zero. This gives:

$$2t_p + \frac{a^2 L_p}{bR_s} = \left[2(t_r + t_p) + \frac{a^2 L_p}{bR_s}\right] \exp\left(-\frac{bR_s t_r}{a^2 L_p}\right). \quad (A.1)$$

Considering the exponential term in this equation, $a^2 L_p/bR_s$ is the time constant of the transformer secondary circuit, and we should expect that, for $i_s(t_r + t_p)$ to be a maximum, this time constant would be several times t_r. If it is, we may write

$$\exp\left(-\frac{bR_s t_r}{a^2 L_p}\right) \doteqdot 1 - \frac{bR_S t_r}{a^2 L_p} \quad (A.2)$$

and substituting this in (A.1) and solving for a, the optimum value of a is found to be

$$a_{opt} = \sqrt{\frac{2bR_s(t_r + t_p)}{L_p}}. \quad (A.3)$$

We must confirm that for this value of a the approximation in (A.2) is valid. Rearranging (A.3),

$$\frac{a_{opt}^2 L_p}{bR_s} = 2(t_r + t_p). \quad (A.4)$$

In practice, t_p would not be less than t_r, and so, from (A.4),

$$a_{opt}^2 L_p / bR_s \geq 4t_r. \quad (A.5)$$

Equation (A.2) is therefore valid.

We must also confirm that (A.3) corresponds to $i_s(t_r + t_p)$ being a maximum and not a minimum. This is done by differentiating (3.5) a second time and noting that for the value of a given by (A.3), the second derivative is negative.

The maximum value of $i_s(t_r + t_p)$ is found by substituting (A.4) in (3.5). This gives:

$$[i_s(t_r + t_p)]_{max} = \frac{k i_{max}}{a_{opt}} \cdot \frac{2(t_r + t_p)}{t_r} \cdot \left\{1 - \exp\left[-\frac{t_r}{2(t_r + t_p)}\right]\right\} \exp\left[-\frac{t_p}{2(t_r + t_p)}\right]. \quad (A.6)$$

From (A.4) and (A.5),

$$\frac{t_r}{2(t_r + t_p)} \leq \frac{1}{4}, \quad (A.7)$$

under which condition

$$1 - \exp\left[-\frac{t_r}{2(t_r + t_p)}\right] \doteqdot \frac{t_r}{2(t_r + t_p)}. \quad (A.8)$$

Substituting (A.8) in (A.6),

$$[i_s(t_r + t_p)]_{max} \doteqdot \frac{k i_{max}}{a_{opt}} \exp\left[-\frac{t_p}{2(t_r + t_p)}\right]. \quad (A.9)$$

Appendix B. Frequency range

Calculation of the ZERO and ONE output signals in Sections 5 and 6 is carried out using Fourier Integral techniques. We are therefore interested in the range of frequencies that these signals contain. Let the lowest frequency of interest be f_1 and the highest f_2, the corresponding values of ω being ω_1 and ω_2 respectively. These values will be used in making certain approximations, and do not represent the limits between which the Fourier transforms are calculated.

Referring to Figs. 8 and 10 we now assume that the input and load currents are sinusoidal, and denote them by I_{in} and I_s respectively. At low frequencies I_s will fall off owing to the shunting effect of kL_s/b (Fig. 10b). Taking f_1 as the frequency at which it has fallen by 3 db,

$$\omega_1 = 2\pi f_1 = \frac{bR_s}{a^2 L_p}. \quad (B.1)$$

For optimum a, as given by (A.3), (B.1) becomes

$$\omega_1 = \frac{1}{2(t_r + t_p)} \quad (B.2)$$

It is clear from Fig. 10b that no similar fall-off occurs at high frequencies; f_2 is therefore determined only by the rise-time of the input pulse. It is given to sufficient accuracy by

$$\omega_2 = 2\pi f_2 = \frac{2\pi}{3t_r} \quad (B.3)$$

When $a = a_{opt}$, ω_2/ω_1 is found from (B.2) and (B.3). It is

$$\frac{\omega_2}{\omega_1} = \frac{4\pi}{3}\left(\frac{t_p}{t_r} + 1\right). \quad (B.4)$$

As mentioned in Section 3, t_p is not normally less than t_r and so, from (B.4)

$$\omega_2/\omega_1 \geq 8.4. \tag{B.5}$$

More often t_p/t_r is in the region of 3, making ω_2/ω_1 about 17.

Appendix C. Input impedance

The impedance Z introduced into a word line by a transformer and its load can be found by analysing the circuit shown in Fig. 10b. It is

$$Z = j\omega L_p\left[1 - k^2 \cdot \frac{(b-1)R_s + j\omega a^2 L_p}{bR_s + j\omega a^2 L_p}\right]. \tag{C.1}$$

When $b \gg k^2/(1-k^2)$ this equation reduces to

$$Z = j\omega L_p(1-k^2). \tag{C.2}$$

In other words, when there are many modules and the corresponding sense windings are connected in parallel, each transformer behaves as though its sense winding were short-circuited. This is also true for smaller numbers of modules, but only at the higher end of the frequency range.

For the single module case ($b = 1$), (C.1) becomes

$$Z = j\omega L_p\left[1 - k^2 \frac{j\omega a^2 L_p}{R_s + j\omega a^2 L_p}\right], \tag{C.3}$$

and, from (B.1) the lowest frequency of interest is given by

$$\omega_1 = \frac{R_s}{a^2 L_p}. \tag{C.4}$$

Substituting (C.4) in (C.3),

$$\frac{Z}{\omega_1 L_p} = \frac{1 + j\frac{\omega}{\omega_1}(1-k^2)}{1 - j\frac{\omega_1}{\omega}}. \tag{C.5}$$

In Fig. 22 this function is plotted against ω/ω_1 for the typical case of $(1-k^2) = 0.1$. For values of ω/ω_1 up to 17 its modulus remains below 2 and its phase angle below 65°. These results are relevant in the study of array resonances (Section 7).

Appendix D. Current transfer ratio in store with 1010 . . . 10111 . . . 110/1010 . . . 10000 . . . 001 pattern

From Fig. 13b the primary current of T_n is given by

$$\frac{I_{p0}}{I_{in}} = \frac{j\omega(n-n'-1)n'CZ}{1 + j\omega(n-n'-1)(n'+1)CZ} \tag{D.1}$$

and the primary current of $T_{n-n'}$ to T_{n-1} by

$$\frac{I_{p1}}{I_{in}} = 1 - \frac{I_{p0}}{I_{in}}. \tag{D.2}$$

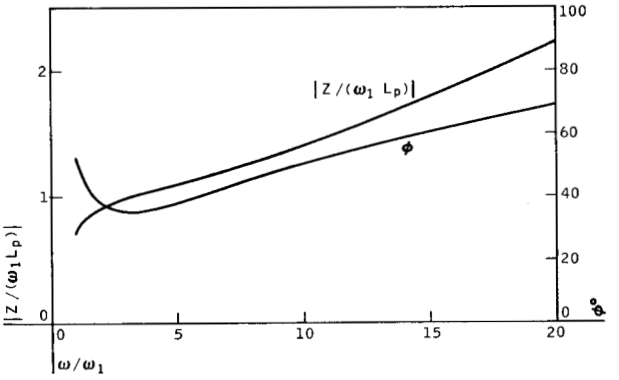


Figure 22 **Modulus and phase angle of $Z/\omega_1 L_p$ in a single module store.** $1 - k^2 = 0.1$

The ratio between the sense amplifier current and the primary current of the corresponding transformer is found from the equivalent circuit in Fig. 10b, noting that the input current to that circuit is now I_{p1} or I_{p0} and the corresponding current through R_s/a^2 is aI_{s1} or aI_{s0}. The ratio is

$$\frac{I_{s1}}{I_{p1}} = \frac{I_{s0}}{I_{p0}} = \frac{k}{a} \cdot \frac{1}{1 + \frac{bR_s}{j\omega a^2 L_p}}. \tag{D.3}$$

The required transfer ratios are found by multiplying (D.1) and (D.2) by (D.3), giving

$$\frac{I_{s0}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \frac{bR_s}{j\omega a^2 L_p}} \cdot \frac{j\omega(n-n'-1)n'CZ}{1 + (n-n'-1)(n'+1)CZ} \tag{D.4}$$

and

$$\frac{I_{s1}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \frac{bR_s}{j\omega a^2 L_p}} - \frac{I_{s0}}{I_{in}}, \tag{D.5}$$

Z being given by (C.1).

Appendix E. Current transfer ratios in store with 111 . . . 110/000 . . . 001 pattern

We first replace the current generator I_{in} in Fig. 15b by two generators A and B, each of the same strength, as shown in Fig. 23. This leaves the currents in the network unchanged. We then calculate the portions of I_{p1} and I_{p0} produced by these two generators in turn. Let the portions produced by A be I_{a1} and I_{a0} respectively, and by B, I_{b1} and I_{b0} respectively.

The output of A divides between the line and Z (representing T_n) in the ratio of their admittances. Thus,

$$I_{a0}/I_{in} = 1/(Y_a Z + 1), \text{ and} \tag{E.1}$$

$$I_{a1}/I_{in} = 1 - I_{a0}/I_{in}, \tag{E.2}$$

Y_a being the admittance of the line looking into terminals aa'. From simple transmission line theory,

$$Y_a = [\tanh \gamma(n-1)]/Z_0 \tag{E.3}$$

where

$$\gamma = \sqrt{Z.j\omega C} \tag{E.4}$$

and

$$Z_0 = \sqrt{\frac{Z}{j\omega C}}. \tag{E.5}$$

Now we consider the response of the circuit to generator B. The impedance looking into terminals bb' is

$$Z_b = Z_0 \frac{Z + Z_0 \tanh \gamma(n-1)}{Z_0 + Z \tanh \gamma(n-1)} \tag{E.6}$$

and the voltage E_b across these terminals is

$$E_b = I_{in} Z_b. \tag{E.7}$$

The terminal current is given by the transmission line equation:

$$I_{b1} = -I_{b0} = I_{in} \cosh \gamma(n-1) - \frac{E_b}{Z_0} \sinh \gamma(n-1), \tag{E.8}$$

which becomes, on substituting from (E.6) and (E.7),

$$\frac{I_{b1}}{I_{in}} = -\frac{I_{b0}}{I_{in}} = \frac{1}{\cosh \gamma(n-1) + \frac{Z}{Z_0} \sinh \gamma(n-1)}. \tag{E.9}$$

From the Superposition Theorem,

$$I_{p0}/I_{in} = I_{a0}/I_{in} + I_{b0}/I_{in} \tag{E.10}$$

and

$$I_{p1}/I_{in} = I_{a1}/I_{in} + I_{b1}/I_{in}. \tag{E.11}$$

Substituting from (E.1), (E.3) and (E.9) into (E.10)

$$\frac{I_{p0}}{I_{in}} = \frac{\cosh \gamma(n-1) - 1}{\frac{Z}{Z_0} \sinh \gamma(n-1) + \cosh \gamma(n-1)} \tag{E.12}$$

and from (E.2), (E.9) and (E.11),

$$I_{p1}/I_{in} = 1 - I_{p0}/I_{in}. \tag{E.13}$$

The ratio of the sense amplifier input current to the transformer primary current is again given by (D.3) and so

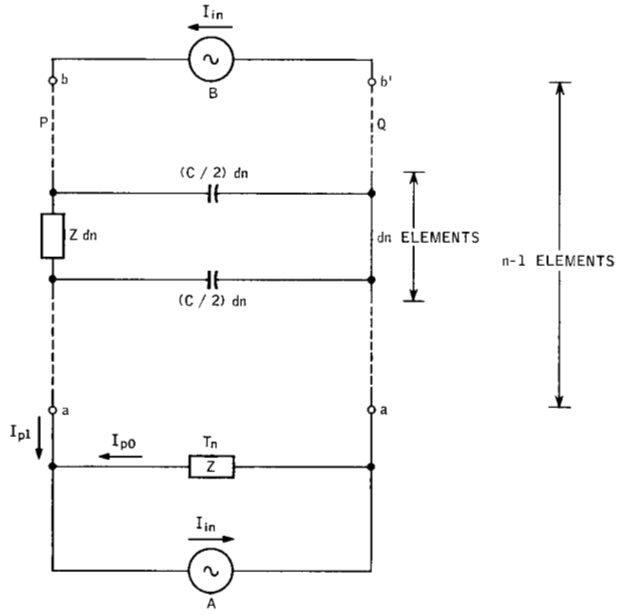


Figure 23 **Equivalent circuit with two generators.**

$$\frac{I_{s0}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \frac{bR_s}{j\omega a^2 L_p}} \cdot \frac{\cosh \gamma(n-1) - 1}{\frac{Z}{Z_0} \sinh \gamma(n-1) + \cosh \gamma(n-1)} \tag{E.14}$$

and

$$\frac{I_{s1}}{I_{in}} = \frac{k}{a} \cdot \frac{1}{1 + \frac{bR_s}{j\omega a^2 L_p}} - \frac{I_{s0}}{I_{in}}. \tag{E.15}$$

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