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Design of a High-Speed Transistor for the ASLT Current Switch

Abstract: The evolution of a high-speed current switch transistor design is described from initial design considerations through final optimization of horizontal geometry. It was found that a very narrow geometry was desirable, in order to produce the desired low base resistance ($\sim$ 40 Ω). Other characteristics of this design include low capacitance, well-controlled emitter forward voltage, and high-frequency cutoff. Compatibility with the SLT form factor assures manufacturability. This transistor when used in ASLT circuits yields circuit delays of 1.8 nsec.

Introduction

The ASLT silicon *npn* transistor has been designed to complement advanced current switch circuit designs and conform to a modified SLT form factor.[1] The evolution of a successful design began with a careful consideration of the parameters desired for current switch circuitry as defined by the circuit designers. The basic requirements were low capacitance, low base resistance, high-frequency cutoff, and very uniform V_{BE} characteristics. The need for good high-frequency response was compatible with the SLT form factor, utilizing its inherent low reactances and proven manufacturability. These requirements and those based on practical experience influenced initial designs.

The designs were evaluated for their ability to meet the parameter values specified in Table 1 and the requirements of circuit performance. Existing devices with suitable impurity profiles and previously specified horizontal geometry would meet all requirements except base resistance. The effect of horizontal geometry on base resistance was evaluated by fabricating devices with different geometries in adjacent rows on several silicon wafers, and comparing their performance. Evaluation of the more advanced low base resistance designs demontrated the desirability of a very narrow geometry.

The final device design utilizes a vertical structure which was evolved throughout the development program in conjunction with an advanced horizontal geometry, both implemented in a glass passivated silicon chip containing 1 to 3 transistors.

Discussion of design

The advantages of n/n^+ epitaxial material are well known for achieving low collector series resistance independently of the choice of collector bulk resistivity. The epitaxial layer thickness of 5 microns was chosen to accommodate the collector junction depth without running into out-diffusion from the n^+ substrate. The resistivity of the epitaxial layer was chosen at 0.1 ohm-cm as a best compromise between minimizing zero-bias and forward-bias collector-base capacitance. As the collector resistivity is increased, the zero-bias capacitance per unit area decreases; this allows a larger collector area to be used. At the same time, however, the forward *I-V* characteristic of the junction changes and minority carriers are injected into the collector region at lower voltages. This results in rapidly increasing effective capacitance at positive voltages. Also, as the collector resistivity was increased beyond 0.2 ohm-cm, it was found that base widening occurred.[2] This increase in electrical base width is due to charge neutralization in the collector, near the collector-base junction, when the current density is comparable to the collector doping. The resulting fall of beta and cutoff frequency were highly undesirable.

When 0.08 ohm-cm material was used, there was a slight reduction in the forward-bias collector capacitance but this was accompanied by an increase in the zero-bias capacitance and a reduction in collector breakdown voltage, BV_{CBO}.

Therefore, the material found most suitable for this

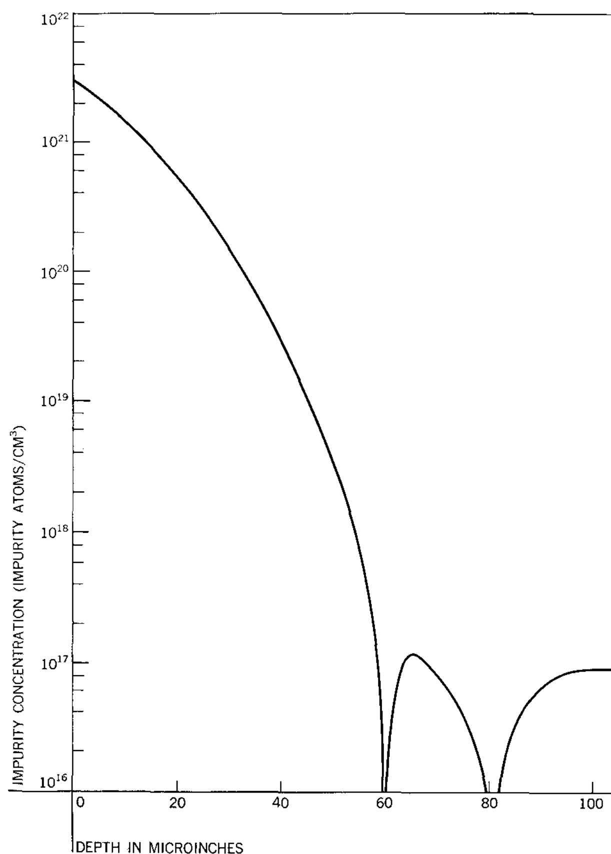


Figure 1 Impurity doping profile.

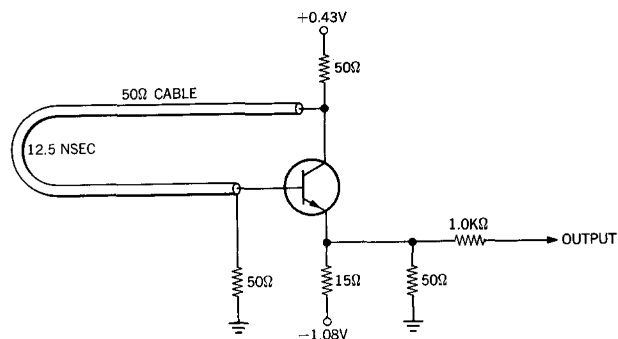


Figure 2 Recirculating loop test circuit.

Table 1 ASLT transistor specifications.

Parameter[a]	*Specification*	*Unit*
BV_{EBO}	3.5 V	6.2 V
BV_{CBO}	6.0 V	20 V
V_{BE} 0.5 mA	0.680–0.730 V	0.690–0.705 V
V_{BE} 16 mA	0.800–0.850 V	0.815–0.835 V
V_{BE} 30 mA	0.840–0.910 V	0.855–0.880 V
H_{FE} 12 mA	25	33
C_{OB} 0.59 V Forward	12 pF	9 pF
Recirculating loop frequency	30.4 Mc	29.9 Mc
r_{bb}	40 Ω	47 Ω

(a) A list of parameter definitions appears on p. 73.

device was 5 micron thick, 0.1 ohm-cm n type, epitaxially grown on a 0.001 ohm-cm n^+ substrate. The diffusions for the base and emitter were variations on processes of known control and reliability. A boron capsule base diffusion was used to insure optimum control of junction depth and surface concentration.[3] An engineering compromise was necessary because the optimum impurity atom concentration (C_0) at the surface for low collector-base capacitance and high beta conflicts with the desire for maximum doping in the base region of the finished device. A C_0 of 5×10^{18} atoms/cm^3 and a junction depth of $X_{jc} = 2\mu$ were found to be the best compromise.

A P_2O_5 emitter diffusion was used to insure surface reliability. The stabilizing effects of a layer of P_2O_5 glass have been reported by Kerr et al.[4] This diffusion resulted in a C_0 of 2×10^{21} and an X_{je} of 1.5μ, leaving a physical base width of 0.5μ. The net doping profile is shown in Fig. 1.

A diffusion schedule was evolved using the above diffusions to fabricate small-area planar transistors. These devices had satisfactory dc characteristics; however, the base resistance was higher than specified. (Typical parameters are shown in Table 1.) Emitter and collector breakdown voltage specifications were low because of inherent low voltage supplies on the logic circuit. V_{BE} was specified at low, intermediate, and high values of current with both minimum and maximum points for universal circuit usage. Collector series resistance was measured by a collector forward bias test (V_{BC}). This test helped control the saturation of input transistors. Forward bias collector capacitance was measured to set an upper limit to the charge the line must supply to on transistors.

High volume production necessitated a quick, reliable method of speed testing before chip mounting. A recirculating loop test as described by Strube et al.[7] was used (Fig. 2 gives the test circuit). By this means, calibration of speeds was held to within ± 10 psec.

An independent specification for the base resistance r_{bb} insured good switching waveforms. Circuit evaluation had confirmed that the switching performance was not satisfactory with the high r_{bb} value and low recirculating frequency; the following design analysis was therefore carried out:

The base resistance can be divided into two basic components. The first, the intrinsic resistance, is inversely proportional to the integral of the base doping as shown in Fig. 1. The effect of geometry on this component is complicated by the non-uniform current distribution under the

emitter. The second component, extrinsic base resistance, is directly proportional to the base sheet resistivity and inversely proportional to the number of unit squares between the emitter edge and the base contact. It thus follows that both components can be reduced if long narrow geometries are used, but altering the vertical structure of the device to decrease base resistance would compromise the dc characteristics. Therefore, horizontal geometries beyond existing art were investigated.

The investigation of new geometries was implemented by using masks made with the fly's eye camera as described by Rudge et al.[5] The use of stop plates to block alternate lenses during alternate exposures enabled the rapid fabrication of masks with different geometries on alternate rows. These alternate-row masks allowed the fabrication of different horizontal designs in alternate adjacent rows of devices on several wafers. Therefore, all variations of material and process were eliminated and direct evaluation of the characteristics of the different geometries could be made. The geometries evaluated are shown in Fig. 3. Note that the areas were held nearly constant to maintain the desired dc characteristics.

The electrical evaluation was done with a test probe consisting of a current switch circuit with one transistor missing. The transistor undeı test was contacted by three small pins protruding from the test module, thereby completing the test circuit shown in Fig. 4. The waveforms of devices from a typical wafer ware shown in Fig. 5. Note that the C design of Fig. 3 follows the input waveform almost identically (Fig. 5c) while the A and B designs of Fig. 3 both have slower rise times, show a breakover, and have a slow exponential approach to the desired level. This break in the waveform occurs near the switching threshold value, making switching time indeterminate.

The C geometry was investigated mathematically by V. Dhaka.[6] It was found that by a meticulous choice of the mathematical model, the actual circuit waveforms observed could be computed, thus substantiating the empirical evaluation. These computations also stressed the value of the narrow emitter of the C design for fast switching. Figure 6 shows the excellent agreement between theoretical and experimental results. Another interesting phenomenon noted was the effect of emitter junction impurity profile. Units with similar base widths and horizontal geometries but with greater emitter gradients switched faster. Dhaka's computations indicate that this is due in part to a decrease in the forward-bias injected minority charge emitter capacitance thus decreasing the $r_e C_e$ time-constant term in the equation for cutoff frequency, F_t. The theoretical vs. experimental f_t results are given in Fig. 7. With the aid of these results a vertical and horizontal design for a specific high-speed current switch transistor was selected.

The current switch configuration uses many common-

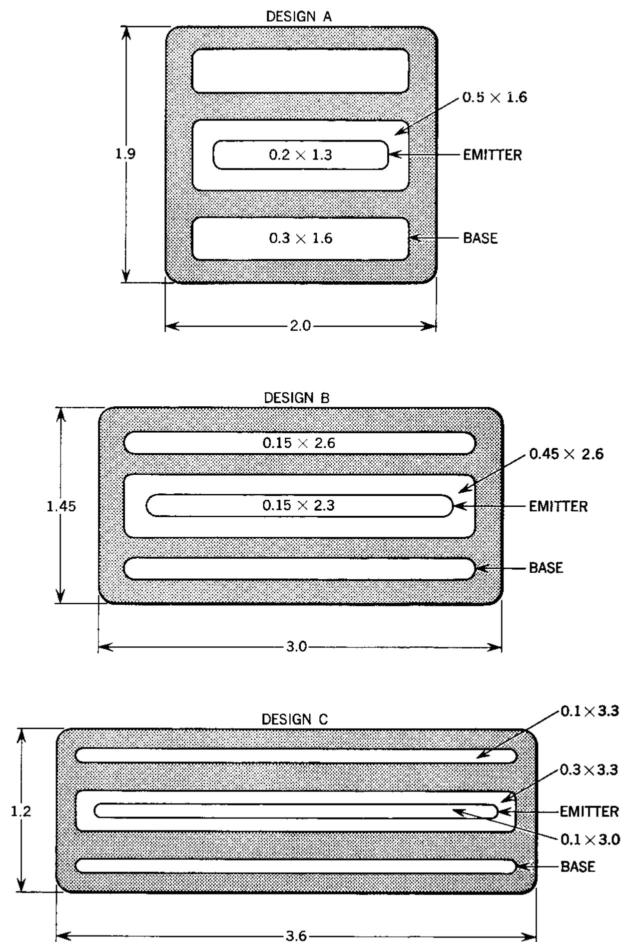
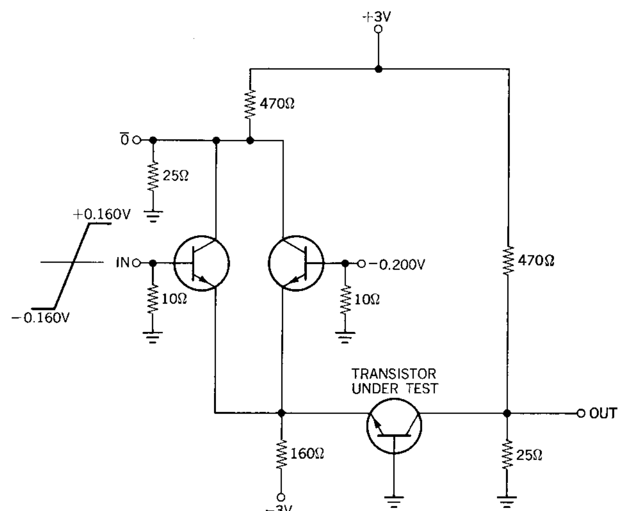
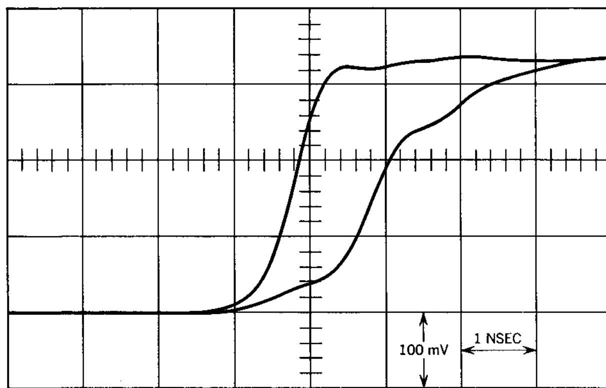


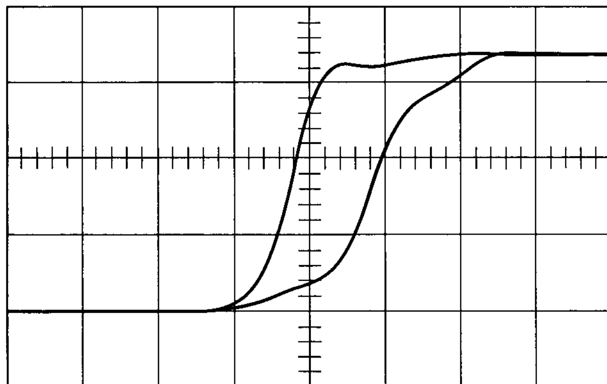
Figure 3 Experimental device geometries.

Figure 4 Switching speed test circuit.

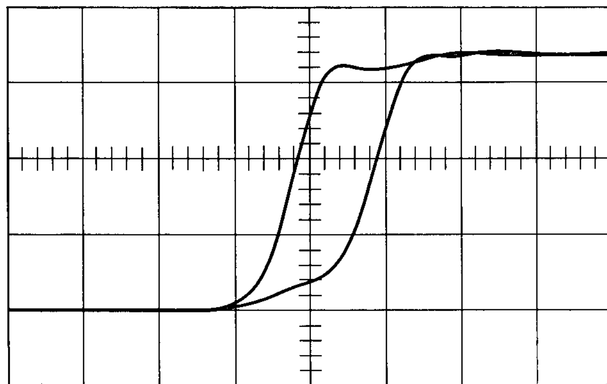




(a)



(b)



(c)

Figure 5 Waveforms showing switching delay and switching response for the device geometries of Fig. 3: (a) design A; (b) design B; (c) design C.

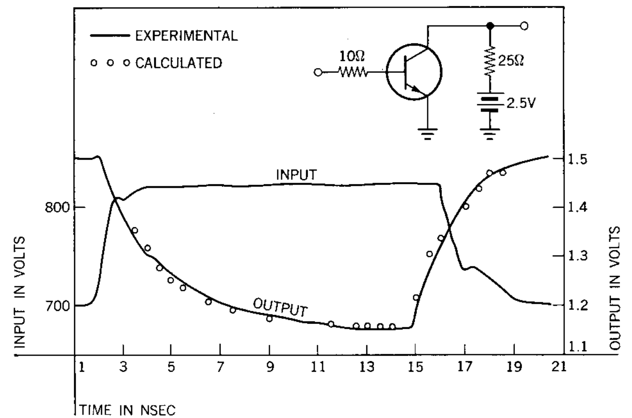
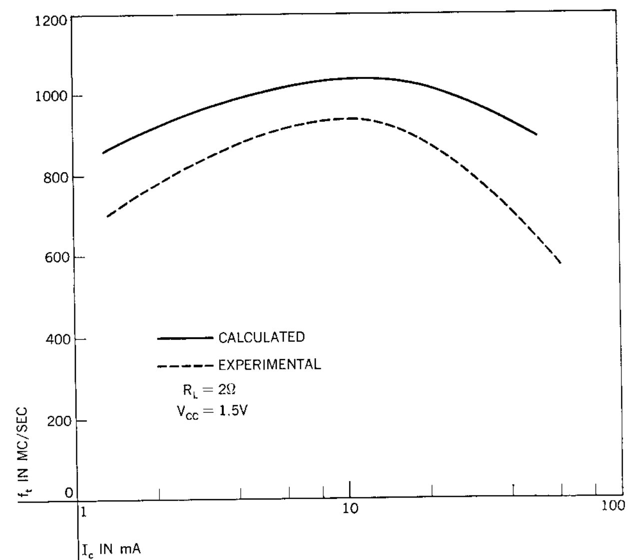


Figure 6 Turn-on and turn-off delay for ASLT transistor (C geometry) in common emitter configuration.

Figure 7 f_t vs. I_c for ASLT transistor (C geometry).



collector transistors. Therefore, common-collector multi-transistor chips could be utilized to increase packaging density.[7] A master chip was designed that presented the option of one or three transistors per chip. Terminal configurations, determined at the glass hole-opening step, were also optional to allow either emitters or bases on the right when viewed from the collector. Two of these unit cells were combined for the three-transistor, common-collector chips.

Summary

A transistor has been empirically designed to fulfill the need for a specific high-speed current switch with closely controlled ac and dc parameters. A design model has been developed that predicts experimental results and will guide future work by means of a computer program. The successful development of future devices, predicted mathematically, will require advanced photoresist capability and improved diffusion control.

Acknowledgment

The authors wish to thank V. A. Dhaka for the use of some of his unpublished computer calculations and the information contained in Fig. 6.

List of parameter definitions

BV_{EBO} Emitter-to-base breakdown voltage, collector open.

BV_{CBO} Collector-to-base breakdown voltage, emitter open.

V_{BE} Base-to-emitter voltage, collector-base "shorted."

H_{FE} Common-emitter current gain.

C_{OB} Collector-to-base capacitance, collector forward-biased.

r_{bb} Base resistance.

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