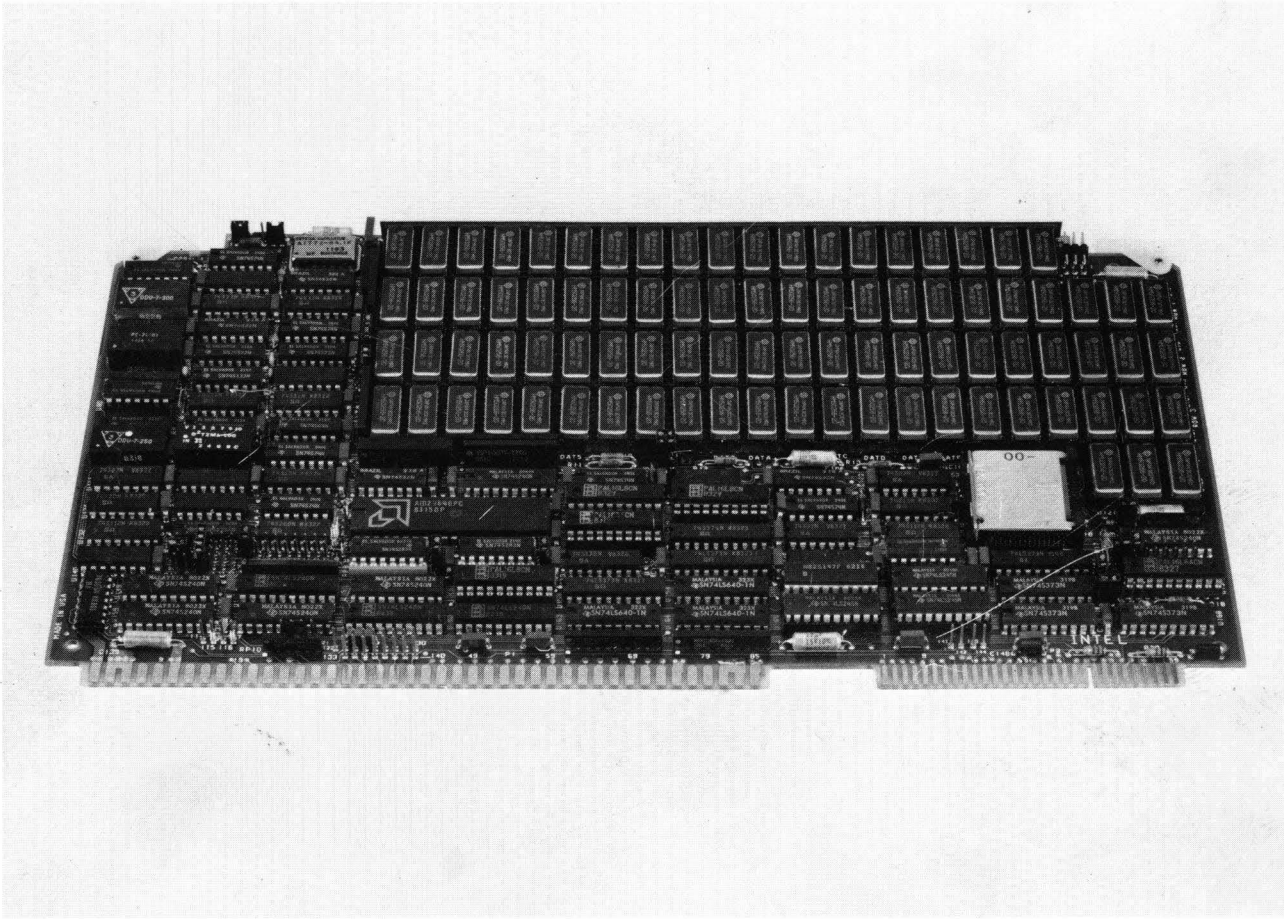
iSBC® 028CX/056CX/012CX/010CX/020CX (CX-SERIES) RAM BOARDS HARDWARE REFERENCE MANUAL



Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Order Number: 145158-003

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REV.	REVISION HISTORY	DATE
-001	Original Issue	9/82
-002	Change Notice (146094-001). Board design changes.	6/83
-003	Update -002. Add 010CX/020CX Boards. Also includes Memory Deselect Option for 012CX/010CX/020CX Boards. Change bars indicate revised or new text/art.	5/84

PREFACE

This manual describes the five "CX-Series" Random Access Memory (RAM) memory boards: the iSBC Ø28CX board, the iSBC Ø56CX board, the iSBC Ø12CX board, the iSBC Ø1ØCX board, and the iSBC Ø2ØCX RAM board. The boards differ only in RAM capacity. Each board features error checking and correcting (ECC) circuitry, MULTIBUS compatibility, and iLBX bus compatibility. This manual explains how to use the boards features in a typical installation. For additional information, the following publications are available from the Intel Literature Department:

- Intel MULTIBUS® Specification, Order Number: 98ØØ683
- Intel iLBX™ Bus Specification, Order Number: 145695
- Intel Microsystems Component Handbook (2 Vol.)
  Order Number: 23Ø843

NOTES

Throughout this manual, a slash (/) following a signal name means that the signal is active-low.

Each RAM board is shipped with a matching set of schematic diagrams. These diagrams should be kept for future reference. The schematic diagrams used in Chapter 5 are for the iSBC 012CX RAM board and are used to represent the iSBC 028CX/056CX/012CX/010CX/020CX RAM Boards. For current and individual board schematics, refer to the set of schematic diagrams shipped with each board.

CONTENTS

CONTENTS (continued)

TABLES

TABLES (continued)

FIGURES

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CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The iSBC CX-Series Random Access Memory (RAM) Boards provide dynamic memory storage capacities of 128K bytes, 256K bytes, 512K bytes, 1Ø24K bytes, and 2Ø48K bytes respectively (Figure 1-1). The boards are compatible in 8-bit or 16-bit systems. The CX-Series of RAM boards uses dynamic RAM devices exclusively, and incorporates error checking and correction (ECC) circuitry on-board. The boards are MULTIBUS and iLBX bus compatible and can be used with battery backup.

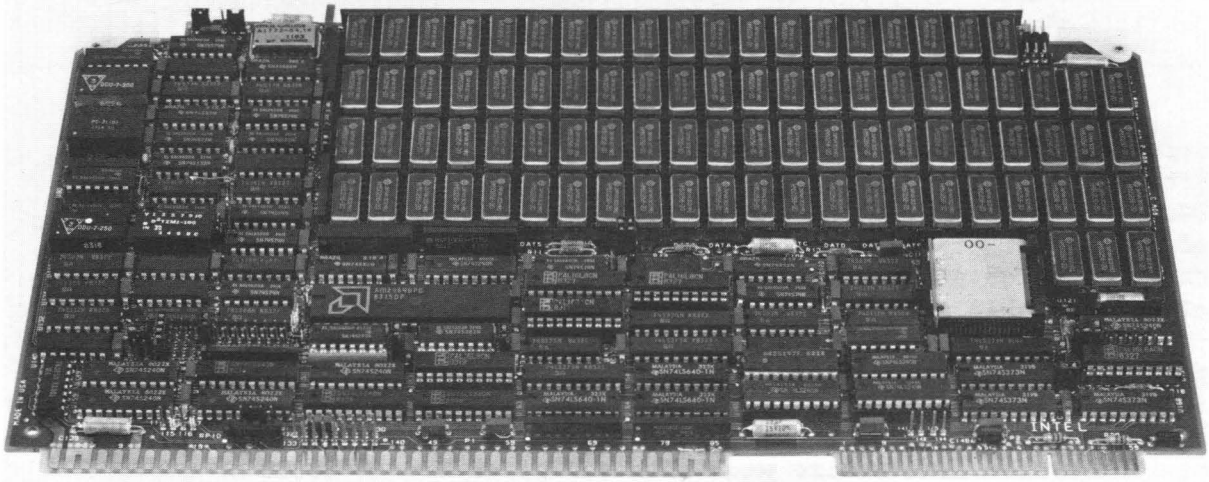

Figure 1-1. iSBC® Ø12CX Random Access Memory Board

1.2 DESCRIPTION

The iSBC CX-Series RAM boards are physically and electrically compatible with the MULTIBUS interface standard as outlined in the INTEL MULTIBUS SPECIFICATION. In addition, the boards feature iLBX bus compatibility. This new Intel Single Board Computer bus is a high-speed extension to the standard MULTIBUS interface. The iLBX bus is described in the INTEL iLBX BUS SPECIFICATION.

The capacity of each RAM board in this series is determined by the type and number of RAM devices on-board. Table 1-1 shows the type and number of devices used for memory and error checking and correction (ECC) on each board. The iSBC Ø28CX, Ø56CX and Ø12CX RAM boards use 64K-bit devices, while the iSBC Ø1ØCX and Ø2ØCX RAM boards use 256K-bit devices.

Table 1-1. Memory and ECC Devices (64K-bit)

Board	Memory (64K-bit)	ECC (64K-bit)
iSBC Ø28CX RAM Board	16	6
iSBC Ø56CX RAM Board	32	12
iSBC Ø12CX RAM Board	64	24
	Memory (256K-bit)	ECC (256K-bit)
iSBC Ø1ØCX RAM Board	32	12
iSBC Ø2ØCX RAM Board	64	24

Error checking and correcting (ECC) is accomplished with the Intel 82Ø6 Error Detection and Correction Unit and other on-board circuitry. The ECC unit allows detection and correction of single-bit errors, detection of double-bit errors and detection of most multiple-bit errors. As used on this series of boards the ECC circuitry can be programmed to correct all correctable errors (double bit and multiple bit errors are not correctable), or to disregard errors. In addition, the board can be programmed to interrupt the processor on any error or only on non-correctable errors.

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independent for the MULTIBUS interface and the iLBX interface. For MULTIBUS operations, system memory is divided into 4-megabyte pages. On-board jumpers assign the board to one of the four pages. Each page is partitioned into 256 blocks of 16K bytes each. The smallest MULTIBUS partition on any board in this series is 16K bytes. Jumpers assign the base address (lowest 16K block) within the selected 4-megabyte page. The 16K-byte block should not cross the 4-megabyte boundary of the board.

The iLBX memory is partitioned into 64K-byte blocks. As shipped, the base address for the iLBX bus memory on the iSBC CX-Series RAM board is set to ØØØØØØH (Hexadecimal). On-board jumpers select the iLBX base address. Refer to Chapter 2 for complete base address jumper information.

All electrical connections to and from the boards are implemented via edge connectors P1, P2 and J1 (See Appendix A). Connector P1 (86-pin) is the MULTIBUS interface connector and P2 (6Ø-pin) is the iLBX bus connector. Connector J1 is used for battery backup control signals.

1.3 DOCUMENTATION SUPPLIED

Each RAM board is shipped with a current set of schematic diagrams. Keep these diagrams for future reference. The schematic diagrams used in Chapter 5 are for the iSBC Ø12CX RAM board and are used to represent the iSBC Ø28CX/Ø56CX/Ø12CX/Ø1ØCX/Ø2ØCX RAM Boards. For individual board schematics, refer to the set of schematic diagrams shipped with the board.

1.4 SPECIFICATIONS

General specifications for the CX-Series RAM boards are listed in Table 1-2. Refer to the INTEL MULTIBUS SPECIFICATION for board AC and DC specifications and MULTIBUS timing information.

Table 1-2. Specifications

BOARD CAPACITY:	
iSBC Ø28CX RAM Board:	128K Bytes (131,Ø72 Bytes)
iSBC Ø56CX RAM Board:	256K Bytes (262,144 Bytes)
iSBC Ø12CX RAM Board:	512K Bytes (524,288 Bytes)
iSBC Ø1ØCX RAM Board:	1Ø24K Bytes (1,Ø48,576 Bytes)
iSBC Ø2ØCX RAM Board:	2Ø48K Bytes (2,Ø97,152 Bytes)
MULTIBUS MEMORY PARTITIONING:	Maximum system RAM size: 16M-bytes
Page Address (4M bytes):	1 of 4 pages, as follows: Ø - 4 Megabytes 4 - 8 Megabytes 8 - 12 Megabytes 12 - 16 Megabytes
Block Address (16K bytes):	
iSBC Ø28CX RAM Board:	8 contiguous 16K-byte blocks (128K bytes)
iSBC Ø56CX RAM Board:	16 contiguous 16K-byte blocks (256K bytes)
iSBC Ø12CX RAM Board:	32 contiguous 16K-byte blocks (512K bytes)
iSBC Ø1ØCX RAM Board:	64 contiguous 16K-byte blocks (1Ø24K bytes)
iSBC Ø2ØCX RAM Board:	128 contiguous 16K-byte blocks (2Ø48K bytes)

Note: Blocks cannot cross 4M-byte page boundary. See Section 2.4.1. for MULTIBUS memory addressing.

Table 1-2. Specifications (continued)

Base Address:	Any 16K-byte boundary with exception of page boundary
REFRESH TIMES:	
Refresh Cycle Time: (between refresh cycles)	15.6 usec.
Refresh Delay Time: (refresh cycle duration)	76Ø nsec. maximum
MULTIBUS ACCESS TIMES:	
Read/Full Write:	35Ø nanoseconds (maximum)
Write Byte:	53Ø nanoseconds (maximum)
Cycle Times:	
Read/Full Write:	46Ø nanoseconds
Write Byte:	835 nanoseconds
Note: When an error is detected, read access time & cycle times are extended by 255 ns (maximum).	
iLBX BUS MEMORY PARTITIONING:	2 blocks of 64K bytes each on iSBC Ø28CX 4 blocks of 64K bytes each on iSBC Ø56CX 8 blocks of 64K bytes each on iSBC Ø12CX 16 blocks of 64K bytes each on iSBC Ø1ØCX 32 blocks of 64K bytes each on iSBC Ø2ØCX
Base Address:	Any 64K-byte boundary
iLBX ACCESS TIMES:	(ASTB/ or DSTB/ to ACK/)
Read/Full Write:	Jumper selectable; see section 2.4.7 and Table 2-12 for details
Write Byte:	44Ø nanoseconds (maximum)
Read Data Access Time:	(ASTB/ to Valid Data on iLBX Bus) 3Ø5 nanoseconds (maximum)
Cycle Times:	
Read/Full Write:	375 nanoseconds (maximum)
Write Byte:	79Ø nanoseconds (maximum)

Table 1-2. Specifications (continued)

MEMORY PROTECTION/BACKUP:	An active low TTL memory protect signal generated by the power supply, (MPRO/) enters the board via J1. This signal disables read/write access to memory thereby protecting data during system power-down. An optional battery can be used to save data. See section 2.4.8.
POWER REQUIREMENTS:	
Voltage:	5VDC ±5%
Current:	iSBC Ø28CX: 6.2A Maximum
	iSBC Ø56CX: 6.35A Maximum
	iSBC Ø12CX: 6.6A Maximum
	iSBC Ø1ØCX: 6.45A Maximum
	iSBC Ø2ØCX: 6.7A Maximum
Battery Current:	iSBC Ø28CX: 2.1A Maximum (Standby mode)
	iSBC Ø56CX: 2.2A Maximum (Standby mode)
	iSBC Ø12CX: 2.4A Maximum (Standby mode)
	iSBC Ø1ØCX: 2.3A Maximum (Standby mode)
	iSBC Ø2ØCX: 2.45A Maximum (Standby mode)
ENVIRONMENTAL REQUIREMENTS:	
Operating Temperature:	Ø°C to 55°C (32°F to 13Ø°F)
Operating Humidity:	To 9Ø% without condensation
PHYSICAL DIMENSIONS:	
Width:	3Ø.48 cm (12.Ø in)
Height:	17.15 cm (6.75 in)
Thickness:	1.27 cm (Ø.5Ø in)
Weight:	
iSBC Ø28CX	469 gm (16.7 oz)
iSBC Ø56CX	532 gm (19.Ø oz)
iSBC Ø12CX	658 gm (23.5 oz)
iSBC Ø1ØCX	532 gm (19.Ø oz)
iSBC Ø2ØCX	658 gm (23.5 oz)

1.5 COMPLIANCE LEVEL: 796 BUS SPECIFICATION (IEEE STANDARD)

All Intel MULTIBUS-compatible boards are designed around guidelines set forth in the 796 BUS SPECIFICATION (IEEE STANDARD - formerly the INTEL MULTIBUS SPECIFICATION). The standard requires that certain board operating characteristics, such as data bus width and memory addressing paths, be clearly stated in the board's printed specifications (i.e.,

reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published 796 BUS SPECIFICATION . It clearly states the board's level of compatibility to the MULTIBUS structure. Refer to the 796 BUS SPECIFICATION or the INTEL MULTIBUS SPECIFICATION for additional information.

The following notation states the iSBC CX-Series RAM board's level of compliance to the 796 BUS SPECIFICATION:

D16 M24 I8

This notation is decoded as follows:

D16 = data path is 8 and/or 16 bits
M24 = memory address path is up to 24 bits
I8 = I/O address path is 8 bits

1.6 iLBX™ BUS COMPLIANCE LEVEL

All Intel iLBX bus-compatible boards are designed around guidelines set forth in the INTEL iLBX BUS SPECIFICATION. The specification requires that certain board operating characteristics, such as data path width, address path width, and other characteristics, be clearly stated in the board's printed specifications (i.e., reference manual). Used properly, this information quickly summarizes the level of compliance the board bears to the published specification. It clearly states the board's level of compatibility to the iLBX bus structure. Refer to the INTEL iLBX BUS SPECIFICATION for more information.

The compliance level for the iSBC CX-Series RAM Boards is as follows:

SL D16

SL indicates the board is a slave board, and D16 indicates a 16-bit data path width.

***

CHAPTER 2
PREPARATION FOR USE

2.1 INTRODUCTION

This chapter provides instructions for preparing the iSBC CX-Series RAM Boards for use in various environments. Included in this chapter are instructions on unpacking and inspection, installation considerations such as physical dimensions and cooling requirements; jumper configurations; and battery back-up configuration.

2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or waterstained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and the packing material for the agent's inspection.

For repair to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order is required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

Save the salvageable shipping cartons and packing material for future use in the event that the board must be shipped.

2.3 INSTALLATION CONSIDERATIONS

Installation considerations such as power, cooling, physical size requirements, and interfacing requirements are outlined in the following paragraphs.

2.3.1 POWER REQUIREMENTS

The power requirements for the RAM boards depend on quantity and type of RAM chips installed onto the RAM boards. See Table 1-2 in Chapter 1 for the various current requirements for each configuration of the RAM boards.

2.3.2 COOLING REQUIREMENTS

The heat dissipation for the RAM boards varies with the configuration of the board; Table 2-1 shows the maximum power dissipation for each configuration. Adequate circulation of air must be provided to prevent a

temperature rise above 55°C (13Ø°F). Typically, a minimum air flow of 2ØØ linear feet per minute at an inlet temperature no higher than 55°C provides enough air circulation to maintain the air temperature around the CX-Series RAM Boards within this limit.

Table 2-1. Heat Dissipation

Board	Dissipation
iSBC Ø28CX	463 gm-cal/minute (1.87 Btu)
iSBC Ø56CX	47Ø gm-cal/minute (1.9Ø Btu)
iSBC Ø12CX	484 gm-cal/minute (1.96 Btu)
iSBC Ø1ØCX	47Ø gm-cal/minute (1.9Ø Btu)
iSBC Ø2ØCX	484 gm-cal/minute (1.96 Btu)

2.3.3 MULTIBUS® INTERFACING REQUIREMENTS

The iSBC CX-Series RAM Boards are designed for installation into a standard Intel iSBC cardcage or into an Intel Microcomputer Development System chassis. The 86-pin edge connector (P1) on the RAM boards provides interfacing to the MULTIBUS structure. Appendix A lists the pin assignments for connector P1.

Edge connector P2 on the RAM boards is used for the iLBX bus control, data, and address lines. MULTIBUS battery back-up signals, and memory protection signals for the RAM boards are routed through connector J1, which is located in the upper right-hand corner of the board. Appendix A lists the pin assignments for connector P2 and connector J1.

2.4 JUMPER CONFIGURATIONS

The iSBC CX-Series RAM board is shipped from the factory with a specific default jumper configuration. The default configuration may require alteration to suit your particular application. The following sections describe the user jumper configurations in their default state and optional states.

2.4.1 MULTIBUS® MEMORY ADDRESSING

The iSBC CX-Series RAM boards support several MULTIBUS addressing modes: 16-bit, 2Ø-bit, and 24-bit addressing. The board is structured to accept 24-bit address words, on MULTIBUS lines ADRØ/ through ADR17/. The two most significant lines (ADR16/ and ADR17/) are used to select a particular 4-megabyte page of addresses. This allows a maximum of 4-megabytes of direct addressing capability, using the remaining 22

address lines (ADR15/ through ADRØ/). When a RAM board is installed in a system, selectable jumpers specify where within the overall 16-megabyte MULTIBUS address space the board is to reside.

Systems with 2Ø address lines should interface directly to MULTIBUS address lines ADRØ/ through ADR13/. This scheme allows addressing of up to 1 megabyte of memory (ØH through ØFFFFFH). Systems with 16 address lines should interface directly to MULTIBUS address lines ADRØ/ through ADRF/. This configuration allows addressing of up to 64K-bytes of memory (ØH through ØØFFFFH).

Four additional address lines are available on connector P2. These are MULTIBUS address lines ADR14/ through ADR17/. Address lines ADR14/ and ADR15/ are used for decoding up to 4 megabytes of memory; lines ADR16/ and ADR17/ are used for full 16-megabyte direct addressing on fully compatible systems.

For universal addressing compatibility, MULTIBUS address lines ADR1Ø/ through ADR17/ are held high (+5VDC) with on-board pull-up resistors. Memory board operation will not be adversely affected if these lines are not used or connected in your system.

In order to select the correct address jumpers for your application, you must consider the overall addressing scheme for this board. MULTIBUS memory address jumpers are configured with two sets of jumpers. The first set selects the particular 4-megabyte page within which the board is to reside. The second set of jumpers selects the base (starting) address for the board, within the selected page. Refer to Section 2.4.1.2 for more information.

When configuring the board for your application first examine the current status of the board. Your application may require changing only one jumper. Typically, the base address selection jumpers will be the most likely to change from application to application. The board is defaulted to the lowest base address (ØØØØØØH in page Ø).

The following sub-sections discuss the four MULTIBUS address jumper sets in more detail. Refer to Figure 2-5 for the physical location of the jumpers on the board.

2.4.1.1 MULTIBUS® Page Address Selection Jumpers

This set of jumpers is used to select the 4-megabyte page in which the board is to reside. MULTIBUS memory allows 16-megabytes, so there are four choices. These choices are shown in Table 2-2. The board will respond only to the code (formed by ADR16/ and ADR17/) which matches the jumper selected page, as described in section 2.4.1. The board is defaulted to page Ø.

Table 2-2. MULTIBUS® Page Select Jumpers

Jumper Pair	Function
7Ø - 76 §	Page Ø (Ø to 4 megabytes)
72 - 78	Page 1 (4 to 8 megabytes)
71 - 77	Page 2 (8 to 12 megabytes)
73 - 79	Page 3 (12 to 16 megabytes)
Note: § = Default Configuration (jumpers installed).	

2.4.1.2 MULTIBUS® Base Address Jumpers

The 4-megabyte memory page selected with the jumpers in Section 2.4.1.1 consists of 256 individual 16-kilobyte blocks. Block Ø is located at the lowest point of the 4-megabyte page and block 255 is located at the highest point in the 4-megabyte page. Figure 2-1 illustrates this concept.

Board capacity determines how many of the 256 blocks are used. The iSBC Ø28CX board uses any 8 contiguous blocks; the iSBC Ø56CX board uses any 16 contiguous blocks; the iSBC Ø12CX board uses any 32 contiguous blocks; the iSBC Ø1ØCX board uses any 64 contiguous blocks; and the iSBC Ø2ØCX board uses any 128 contiguous blocks. Refer to Figure 2-1.

The base address is defined as the starting point of the lowest block you select. Board memory will then continue upward for the number of contiguous blocks according to capacity. Any 16K-byte block can be selected for a base address. The base address is set by creating an eight-bit binary value with the base address selection jumpers. Installing a jumper in one of the digits equals a binary 1; conversely, absence of a jumper equals a binary Ø. Table 2-3 correlates the jumpers to their binary equivalents.

A binary value of ØØØØØØØØ selects the first 16K-byte block and a binary value of 11111111 (255 decimal) selects the last 16k byte block. Any of the 256 blocks may be selected as the base address. The start of block Ø corresponds to hexadecimal address ØØØØØØH and the end of block 255 corresponds to 3FFFFFH.

The selected memory space cannot cross a 4-megabyte page boundary. Any 16K-byte blocks extending into the next 4-megabyte page, will wrap around to the beginning of the memory page in which the base address block exists. For example, if you want your base address to be at block 17,

you would install jumpers between posts 47 - 63 and 51 - 67. This is a binary value of ØØØ1ØØØ1 or 17 decimal. Assuming you had a iSBC Ø28CX board (128K-bytes capacity), your address space would extend from the first byte in block 17 through the last byte in block 24 for a total of eight 16K-byte blocks. This is equivalent to addresses 44ØØØH - 63FFFH.

NOTE

Remember that on-board RAM is shared by MULTIBUS memory and iLBX bus memory. Because of this sharing, we recommend that the address space selected for each bus fully overlap. For example, if the MULTIBUS base address is set to 512K bytes, then the iLBX bus base address should also be set to 512K bytes. If the memory is partially overlapped, or not overlapped at all, iLBX bus data could be written into different MULTIBUS locations under certain conditions.

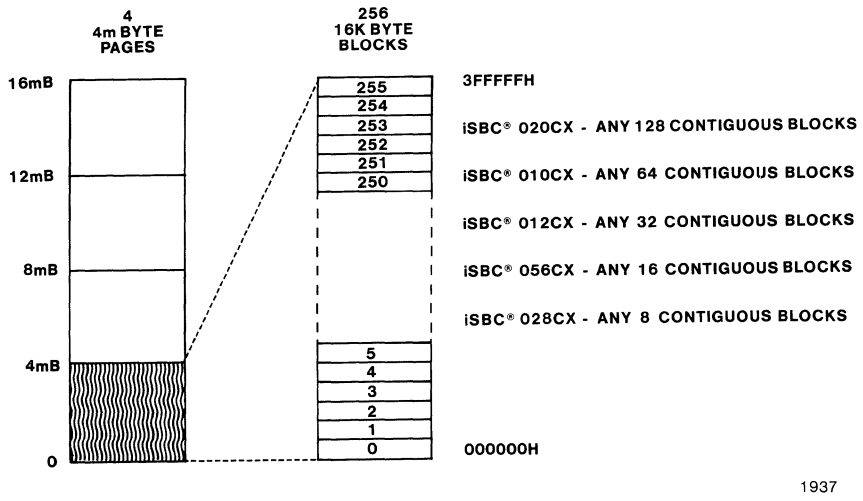

Figure 2-1. MULTIBUS® Page and Base Address Concept

Another example of base address selection on an iSBC Ø12CX board is shown in Figure 2-2. See Section 2.4.1.4 for iLBX bus addressing jumper configurations.

Table 2-3. MULTIBUS® Base Address Selection Jumpers

Jumper Pair	Function
44 - 6Ø	Base Address Bit 7 (MSB)
45 - 61	Base Address Bit 6
46 - 62	Base Address Bit 5
47 - 63	Base Address Bit 4
48 - 64	Base Address Bit 3
49 - 65	Base Address Bit 2
5Ø - 66	Base Address Bit 1
51 - 67	Base Address Bit Ø (LSB)
Note: Default configuration is all jumpers out (removed). (Jumper IN = 1; Jumper OUT = Ø)	

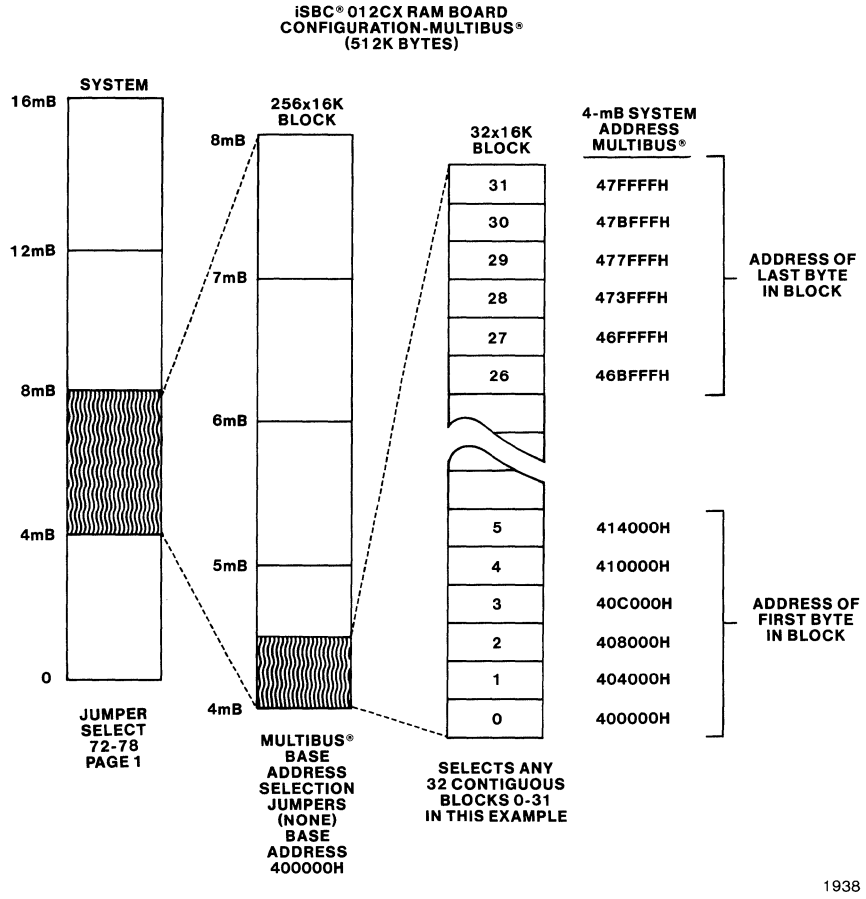

Figure 2-2. MULTIBUS® Base Address Example

2.4.1.3 iLBX™ Bus Memory Addressing

The iLBX bus memory address space consists of 256 contiguous blocks of 64K bytes each. This is a total of 16 megabytes of memory. As shipped from the factory, each board is configured so that the board starts at address ØØØØØØH, and continues upward for the number of contiguous 64K-byte blocks allowed for its capacity. The iSBC Ø28CX board occupies 128K bytes (ØØØØØØH to 1FFFFH); the iSBC Ø56CX board occupies 256K bytes (ØØØØØØH to 3FFFFH); the iSBC Ø12CX board occupies 512K bytes (ØØØØØØH to 7FFFFH); the iSBC Ø1ØCX board occupies 1Ø24K bytes (ØØØØØØH to FFFFFH); and the iSBC Ø2ØCX board occupies 2Ø48K bytes (ØØØØØØH to 1FFFFFH).

2.4.1.4 iLBX™ Bus Base Address And Address Range Jumpers

The iLBX base address and address range is a function of on-board Programmed Array Logic (PAL) device U158 and the iLBX base address and range jumpers selected. Three jumpers are used to select the iLBX base address and address range. The default iLBX base address for the CX-Series boards is zero (ØØØØØØH).

The memory boards examine iLBX address lines AB1Ø - AB17 to determine if the address on the iLBX bus refers to on-board memory. If more than one iLBX memory board is used in your system, ensure that the address ranges of the boards do not cause memory space overlapping. There are 21 pre-programmed address ranges for the iSBC Ø28CX/Ø56CX boards; 28 for the iSBC Ø12CX board; and 14 for the iSBC Ø1ØCX/Ø2ØCX boards.

The pre-programmed PAL can be replaced with the users PAL, which can then be programmed to provide additional address ranges for the board. See Appendix B for current PAL code.

Tables 2-4, 2-5, 2-6, 2-7, and 2-8 correlate the jumper connections to the iLBX address range selection for the iSBC CX-Series RAM Boards.

Table 2-4. iLBX™ Bus Address Range Jumpers

iSBC® Ø28CX 128K RAM Board				
Jumpers	1Ø6-1Ø7 § 1Ø9-11Ø §	1Ø6-1Ø7 11Ø-111	1Ø7-1Ø8 1Ø9-11Ø	1Ø7-1Ø8 11Ø-111
91-99 §	ØØØØØØ-Ø1FFFF	ØEØØØØ-ØFFFFF	1CØØØØ-1DFFFF	User Programmable w/ User's PAL
92-1ØØ	Ø2ØØØØ-Ø3FFFF	1ØØØØØ-11FFFF	1EØØØØ-1FFFFF	
93-1Ø1	Ø4ØØØØ-Ø5FFFF	12ØØØØ-13FFFF	2ØØØØØ-21FFFF	
94-1Ø2	Ø6ØØØØ-Ø7FFFF	14ØØØØ-15FFFF	22ØØØØ-23FFFF	
95-1Ø3	Ø8ØØØØ-Ø9FFFF	16ØØØØ-17FFFF	24ØØØØ-25FFFF	
96-1Ø4	ØAØØØØ-ØBFFFF	18ØØØØ-19FFFF	26ØØØØ-27FFFF	
97-1Ø5	ØCØØØØ-ØDFFFF	1AØØØØ-1BFFFF	28ØØØØ-29FFFF	

Notes: § - Indicates default jumper.

All addresses in Hexadecimal.

Table 2-5. iLBX™ Bus Address Range Jumpers

iSBC® Ø56CX 256K RAM Board				
Jumpers	1Ø6-1Ø7 § 1Ø9-11Ø §	1Ø6-1Ø7 11Ø-111	1Ø7-1Ø8 1Ø9-11Ø	1Ø7-1Ø8 11Ø-111
91-99 §	ØØØØØØ-Ø3FFFF	1CØØØØ-1FFFFF	38ØØØØ-3BFFFF	User Programmable w/ User's PAL
92-1ØØ	Ø4ØØØØ-Ø7FFFF	2ØØØØØ-23FFFF	3CØØØØ-3FFFFF	
93-1Ø1	Ø8ØØØØ-ØBFFFF	24ØØØØ-27FFFF	4ØØØØØ-43FFFF	
94-1Ø2	ØCØØØØ-ØFFFFF	28ØØØØ-2BFFFF	44ØØØØ-47FFFF	
95-1Ø3	1ØØØØØ-13FFFF	2CØØØØ-2FFFFF	48ØØØØ-4BFFFF	
96-1Ø4	14ØØØØ-17FFFF	3ØØØØØ-33FFFF	4CØØØØ-4FFFFF	
97-1Ø5	18ØØØØ-1BFFFF	34ØØØØ-37FFFF	5ØØØØØ-53FFFF	

Notes: § - Indicates default jumper.

All addresses are in Hexadecimal.

Table 2-6. iLBX™ Bus Address Range Jumpers

iSBC® Ø12CX 512K RAM Board				
Jumpers	1Ø6-1Ø7 § 1Ø9-11Ø §	1Ø6-1Ø7 11Ø-111	1Ø7-1Ø8 1Ø9-11Ø	1Ø7-1Ø8 11Ø-111
91-99 §	ØØØØØØ-Ø7FFFF	38ØØØØ-3FFFFF	7ØØØØØ-77FFFF	ØØØØØØ-Ø5FFFF ¶
92-1ØØ	Ø8ØØØØ-ØFFFFF	4ØØØØØ-47FFFF	78ØØØØ-7FFFFF	Ø1ØØØØ-Ø8FFFF
93-1Ø1	1ØØØØØ-17FFFF	48ØØØØ-4FFFFF	8ØØØØØ-87FFFF	Ø2ØØØØ-Ø9FFFF
94-1Ø2	18ØØØØ-1FFFFF	5ØØØØØ-57FFFF	88ØØØØ-8FFFFF	Ø3ØØØØ-ØAFFFF
95-1Ø3	2ØØØØØ-27FFFF	58ØØØØ-5FFFFF	9ØØØØØ-97FFFF	Ø4ØØØØ-ØBFFFF
96-1Ø4	28ØØØØ-2FFFFF	6ØØØØØ-67FFFF	98ØØØØ-9FFFFF	Ø5ØØØØ-ØCFFFF
97-1Ø5	3ØØØØØ-37FFFF	68ØØØØ-6FFFFF	AØØØØØ-A7FFFF	Ø6ØØØØ-ØDFFFF

Notes: § - Indicates default jumper.

¶ - Indicates this configuration is memory deselected, the full memory capacity is not addressed.

All addresses are in Hexadecimal.

Table 2-7. iLBX™ Bus Address Range Jumpers

iSBC® Ø1ØCX 1M RAM Board				
Jumpers	1Ø6-1Ø7 § 1Ø9-11Ø §	1Ø6-1Ø7 11Ø-111	1Ø7-1Ø8 1Ø9-11Ø	1Ø7-1Ø8 11Ø-111
91-99 §	ØØØØØØ-ØFFFFF	User Programmable w/ User's PAL	User Programmable w/ User's PAL	ØØØØØØ-ØCFFFF ¶
92-1ØØ	1ØØØØØ-1FFFFF			ØØØØØØ-ØDFFFF ¶
93-1Ø1	2ØØØØØ-2FFFFF			ØØØØØØ-ØEFFFF ¶
93-1Ø2	3ØØØØØ-3FFFFF			ØCØØØØ-1BFFFF
95-1Ø3	4ØØØØØ-4FFFFF			1ØØØØØ-1FFFFF
96-1Ø4	5ØØØØØ-5FFFFF			14ØØØØ-23FFFF
97-1Ø5	6ØØØØØ-6FFFFF			18ØØØØ-27FFFF

Notes: § - Indicates default jumper.

¶ - Indicates this configuration is memory deselected, the full memory capacity is not addressed.

All addresses are in Hexadecimal.

Table 2-8. iLBX™ Bus Address Range Jumpers

iSBC® Ø2ØCX 2M RAM Board				
Jumpers	1Ø6-1Ø7 § 1Ø9-11Ø §	1Ø6-1Ø7 11Ø-111	1Ø7-1Ø8 1Ø9-11Ø	1Ø7-1Ø8 11Ø-111
91-99 §	ØØØØØØ-Ø1FFFFF	User Programmable w/ User's PAL	User Programmable w/ User's PAL	ØØØØØØ-ØDFFFF ¶
92-1ØØ	2ØØØØØ-Ø3FFFFF			Ø1ØØØØ-2ØFFFF
93-1Ø1	4ØØØØØ-Ø5FFFFF			Ø2ØØØØ-21FFFF
94-1Ø2	6ØØØØØ-Ø7FFFFF			1ØØØØØ-2FFFFF
95-1Ø3	8ØØØØØ-Ø9FFFFF			Ø8ØØØØ-9FFFFF
95-1Ø4	AØØØØØ-ØBFFFFF			ØAØØØØ-BFFFFF
97-1Ø5	CØØØØØ-ØDFFFFF			ØCØØØØ-DFFFFF

Notes: § - Indicates default jumper.

¶ - Indicates this configuration is memory deselected, the full memory capacity is not addressed.

All addresses in Hexadecimal.

2.4.1.5 Memory Deselect (iSBC® 012CX/010CX/020CX RAM Boards Only)

The iSBC Ø12CX/Ø1ØCX/Ø2ØCX boards allow deselection of portions of their upper addressed memory. This allows the memory size of a board to look smaller than it physically is. This option, however, forces the base address of the board to zero. One possible use for the deselected address space is a memory location for other memory-mapped boards. While it is possible to deselect the MULTIBUS independently from the iLBX bus, it is not recommended due to the deselected memory addresses being accessible only by the iLBX bus.

To deselect memory from the iLBX bus, choose the jumper options for deselect listed in Table 2-6, 2-7 or 2-8 for the iSBC Ø12CX/Ø1ØCX/Ø2ØCX RAM Boards. For example, on an iSBC Ø12CX board, choosing the jumper option of 1Ø7-1Ø8 and 11Ø-111 along with 91-99 sets-up a base address of ØH with the upper 128K bytes deselected. This causes the board to respond only to memory addresses ØH through 5FFFFH.

Deselection of memory from the MULTIBUS system is accomplished differently. First, the MULTIBUS Deselection option must be selected by the following jumper modifications:

Remove Jumper: 29-34

Install Jumper: 33-34

Next, the size of the memory segment deselected is defined by the MULTIBUS Address Range Selection jumpers. The size is set by creating an eight-bit binary value with the address range selection jumpers. The size of the memory segment deselected is equal to the eight-bit binary value, plus one, in 16K-byte blocks. In this configuration, a jumper installed is a Ø, and a jumper removed is a 1 (see table 2-9).

For example, performing the following jumper modifications sets-up a MULTIBUS address range of ØØØØØØH through 5FFFFH on an iSBC Ø12CX board:

Remove Jumper: 34-29

Install Jumper: 34-33
48-64
47-63
46-62
45-61
44-6Ø

In this example, the eight-bit binary value ØØØØØ111 is formed on the Address Range Selection Jumpers. This deselects the top 8 (7 plus 1) 16K-byte segments, or 128K bytes total. This causes the board to respond only to memory addresses ØØØØØØH through 5FFFFH. Figure 2-3 shows the deselect option along with the jumper modifications. Once again, remember that memory deselected boards always start at a base address of zero.

Table 2-9. MULTIBUS® Address Range Selection Jumpers with Deselect Option (Jumper 33-34)

Jumper Pair		Function
(MSB)	44-6Ø	Base Address Bit 7
	45-61	Base Address Bit 6
	46-62	Base Address Bit 5
	47-63	Base Address Bit 4
	48-64	Base Address Bit 3
	49-65	Base Address Bit 2
	5Ø-66	Base Address Bit 1
(LSB)	51-67	Base Address Bit Ø
Note: Jumper IN = Ø; Jumper OUT = 1.		

2.4.2 ECC I/O ADDRESS SELECTION

The Error Checking and Correction (ECC) circuitry communicates with the processor board through a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The iSBC CX-Series RAM board is shipped with a Programmed Array Logic (PAL) device (U152) which allows selecting one of nine possible addresses for the I/O port. The actual selection is done by jumper configuration. If your application requires an I/O address which is not listed in Table 2-1Ø, the PAL at location U152 must be replaced and the user's PAL reprogrammed (refer to Appendix B).

Three sets of jumpers are used to select the desired I/O address that the board will recognize. Table 2-1Ø illustrates the nine possible addresses and indicates the default I/O address (Ø1CØH). The table shows how to assign one of the nine addresses to the board, using the three sets of jumpers.

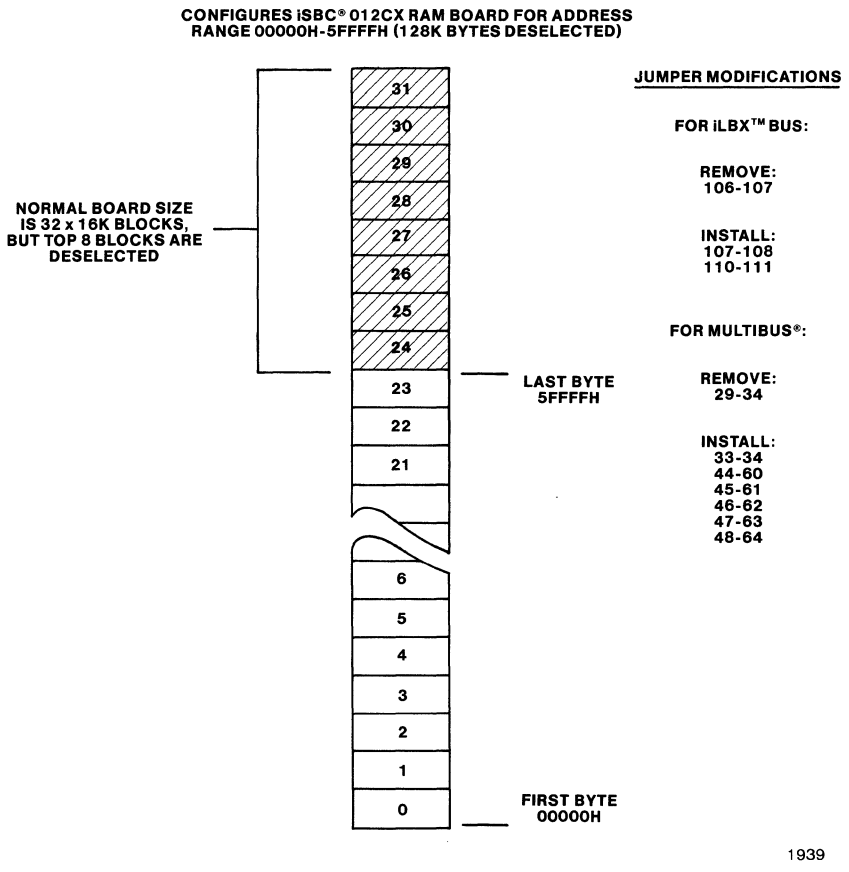

Figure 2-3. iSBC® Ø12CX RAM Board with Deselect Option (Example)

Table 2-1Ø. I/O Address Jumpers

Jumpers (IN)	86-87 §		85-86	
	83-84 §	82-83	83-84	82-83
39-55 § 4Ø-56 41-57 42-58	Ø1CØH 41CØH 81CØH C1CØH	Ø1C1H 41C1H 81C1H C1C1H	ØØ4ØH	User Programmable
Note: § - Indicates default jumper configuration.				

2.4.3 iLBX™ BUS INTERFACE ADDRESS STROBE JUMPER

The memory board is shipped from the factory configured for iLBX bus and MULTIBUS operation. If your application is MULTIBUS-ONLY, install the following jumper:

9Ø - 98

2.4.4 iLBX™ BUS SPEED SELECTION JUMPER

In the default configuration (as-shipped), the iLBX Bus interface on the CX-Series boards operates in fast mode. In fast mode, the iLBX cycle starts after ASTB/ becomes active. In slow mode, an iLBX cycle is not started until both ASTB/ and DSTB/ have become active. To enable the slow mode, perform the following jumper modifications:

Remove Jumper: 1Ø-11
Install Jumper: 11-12

2.4.5 INTERRUPT LEVEL SELECTION JUMPERS

The on-board ECC circuitry will generate an interrupt as specified in Section 3.2. The interrupt can be placed on a jumper-selected MULTIBUS interrupt line. Jumpers are used to specify the interrupt level and MULTIBUS line. The default setting for the interrupt is INTØ/. Table 2-11 provides a list of all the interrupt lines and jumpers. Push-on jumper headers are used to select the interrupt level, as shown in Table 2-11.

Whenever an interrupt is generated the on-board indicator lamp (LED) will illuminate. This lamp can be used for test and diagnostic purposes.

Table 2-11. Interrupt Level Selection Jumpers

Jumper Pair	Level	MULTIBUS® Pin
13Ø - 14Ø §	INTØ/	P1 - 41
129 - 139	INT1/	P1 - 42
128 - 138	INT2/	P1 - 39
127 - 137	INT3/	P1 - 4Ø
126 - 136	INT4/	P1 - 37
125 - 135	INT5/	P1 - 38
124 - 134	INT6/	P1 - 35
123 - 133	INT7/	P1 - 36
Note: § - Indicates default jumper configuration; jumper installed.		

2.4.6 EXTERNAL REFRESH (REFRQST) JUMPER

The iSBC CX-Series RAM boards are configured at the factory for on-board refresh. If an external, off-board refresh is needed for test purposes, it is possible to disable the on-board refresh circuitry. The iLBX bus cannot be used if an external refresh is employed as the refresh pins are defined by the iLBX connector. To enable external refresh, perform the following modifications:

a. Remove jumper 5 - 6.
b. Install jumper 4 - 5.
c. Install jumper 141 - 142.
d. Connect the external refresh signal to pin 4Ø of connector P2.

2.4.7 iLBX™ BUS ACKNOWLEDGE TIME SELECTION JUMPERS

The iSBC CX-Series RAM boards acknowledge time for iLBX bus requests can be optimized for a given master-slave (host board, CX-Series board) application. Table 2-12 provides acknowledge times for the CX-Series boards and their associated jumper connections. Figure 2-4 illustrates the timing waveforms for the iLBX Bus Acknowledge activity.

In optimized mode, the master-slave timing relationship is selected for Read cycles. Refer to the INTEL iLBX BUS SPECIFICATION for additional details on optimized operation. Also refer to the Acknowledge Acceptance Times for the host board as well as Figure 2-4 and Table 2-12 to select the optimum acknowledge time for your given application.

The iLBX Read cycle is started by ASTB/ (or DSTB/ if in slow mode). The time interval between ASTB/ (or DSTB/) from the master and the acknowledge signal (ACK/) from the slave is defined as T1, and is jumper selectable to meet the masters minimum wait-state requirements. The minimum time for T1 must be greater than the maximum value of ASTB/ to DSTB/ + 1Ø nanoseconds.

T1 and T2 Times: See Table 2 - 12.

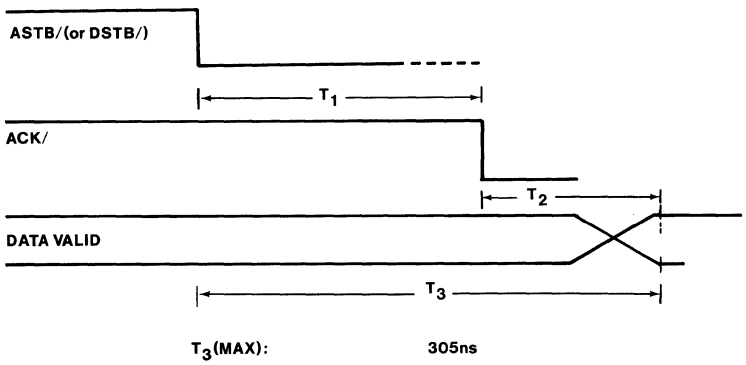

Figure 2-4. iLBX™ Bus Acknowledge Time Waveforms

The maximum time from ACK/ to when valid data is present is defined as T2, and is also a function of the jumpers selected. This time must also match the masters timing requirements, as the master cannot read data before it is valid.

The maximum time from ASTB/ to data valid is defined as T3 and is a maximum of 3Ø5 nanoseconds. T3 is independent of ACK/ timing and is not jumper selectable.

Table 2-12. Acknowledge Time Selection Jumpers

Jumpers	T1 Min	T1 Max	T2 Max
38 - 68 and:			
17 - 16	65ns	117ns	212ns
17 - 7	82ns	138ns	193ns
17 - 9	92ns	148ns	183ns
17 - 8	1Ø1ns	159ns	174ns
68 - 54 ¶	135ns	196ns	14Øns
43 - 59 § and:			
68 - 69 §	2Ø6ns	274ns	69ns
68 - 36	23Øns	3Ø1ns	45ns
68 - 74	254ns	327ns	21ns
68 - 75	278ns	353ns	-3ns
68 - 53	3Ø1ns	379ns	-26ns
68 - 37	325ns	4Ø6ns	-5Øns

Notes: § - Default jumper configuration.

¶ - Installing this jumper only, gives the times stated.

A negative time indicates that T2 is occurring after data is valid.

2.4.8 BATTERY BACK-UP AND MEMORY SAVE JUMPERS

In systems employing a battery back-up and memory save feature, the user must interface to connector J1. The system power supply must generate some type of power-failure signal, for full MULTIBUS compatibility. Intel power supplies such as the iSBC 645 Power Supply generate an AC Low signal (ACLO/), and a Memory Protect (MPRO/) signal for this purpose. The timing of these two signals is critical for implementing a battery back-up scheme. The MPRO/ signal is used by the RAM boards to prevent access to memory during a power-down condition. The ACLO/ signal is not used by the RAM boards, but could be used by the CPU board. Refer to the INTEL MULTIBUS SPECIFICATION for guidelines on battery back-up schemes.

Connector J1 is referenced in the INTEL iLBX BUS SPECIFICATION and the battery back-up signals are supported by the iSBC CX-Series boards. Connect the appropriate battery back-up, memory protect, and other control lines to the connector, as listed in Appendix A.

NOTE

Data integrity is not guaranteed during an active memory access cycle in which a memory protect signal (MPRO/) is generated by the power supply.

When battery back-up power is to be installed for use with the RAM board, remove the following factory installed jumpers:

22 - 23
24 - 25
8Ø - 81
88 - 89

Battery backup power enters the board at J1-1 and J1-3 on the auxiliary connector. Ground is on J1-2 and J1-4. See Appendix A for connector J1 pin assignments.

CAUTION

Always remove both battery back-up and system power from the RAM boards before installing or removing the boards from a system cardcage. Failure to do so could result in damage to the boards.

2.5 BOARD INSTALLATION

The iSBC CX-Series RAM Boards are compatible with all MULTIBUS backplanes and cardcages. For iLBX bus compatibility, a special iLBX connector must be used to link the processor board to the memory board. The iLBX bus uses connector P2 and may not be compatible with earlier configurations of connector P2. Refer to Section 2.4.8 for battery backup information.

2.6 FACTORY DEFAULT JUMPERS

For each of the iSBC CX-Series boards, Table 2-13 provides a list of the jumpers that are installed at the factory. Figure 2-5 provides a jumper post location diagram of the boards.

Table 2-13. Factory Installed Jumpers

Jumper	Function	ØØ28CX	ØØ56CX	ØØ12CX	ØØ1ØCX	ØØ2ØCX
ØØ1 - ØØ2	Refresh	I	I	I	I	I
ØØ5 - ØØ6	Refresh	I	I	I	I	I
Ø1Ø - Ø11	SPRQT	I	I	I	I	I
Ø13 - Ø14	CAS Timing	I	I	I	I	I
Ø19 - Ø2Ø	R/C Timing	I	I	I	I	I
Ø22 - Ø23	+5VB	I	I	I	I	I
Ø24 - Ø25	+5VB	I	I	I	I	I
Ø26 - Ø3Ø	Board Size	N	I	I	I	I
Ø26 - Ø31	Board Size	I	N	N	N	N
Ø27 - Ø32	Board Size	I	I	I	I	N
Ø27 - Ø3Ø	Board Size	N	N	N	N	I
Ø28 - Ø33	Board Size	I	I	N	N	N
Ø28 - Ø35	Board Size	N	N	I	I	I
Ø29 - Ø34	Deselect	I	I	I	I	I
Ø39 - Ø55	I/O Address	I	I	I	I	I
Ø43 - Ø59	iLBX ACK	I	I	I	I	I
Ø68 - Ø69	iLBX ACK	I	I	I	I	I
Ø7Ø - Ø76	1 MB Page	I	I	I	I	I
Ø8Ø - Ø81	+5VB	I	I	I	I	I
Ø83 - Ø84	I/O Address	I	I	I	I	I
Ø86 - Ø87	I/O Address	I	I	I	I	I
Ø88 - Ø89	+5VB	I	I	I	I	I
Ø91 - Ø99	iLBX BDSEL	I	I	I	I	I
1Ø6 - 1Ø7	iLBX BDSEL	I	I	I	I	I
1Ø9 - 11Ø	iLBX BDSEL	I	I	I	I	I
114 - 117	Board Size	I	N	N	N	N
155 - 117	Board Size	N	N	N	I	I
116 - 117	Board Size	N	I	I	N	N
118 - 12Ø	Board Size	I	I	N	I	N
119 - 12Ø	Board Size	N	N	N	N	I
12Ø - 121	Board Size	N	N	I	N	N
13Ø - 14Ø	INT Ø/	I	I	I	I	I
145 - 146	Test Only	I	I	I	I	I
148 - 149	ARBTR Time	I	I	I	I	I

Notes: I = jumper installed; N = jumper not installed.

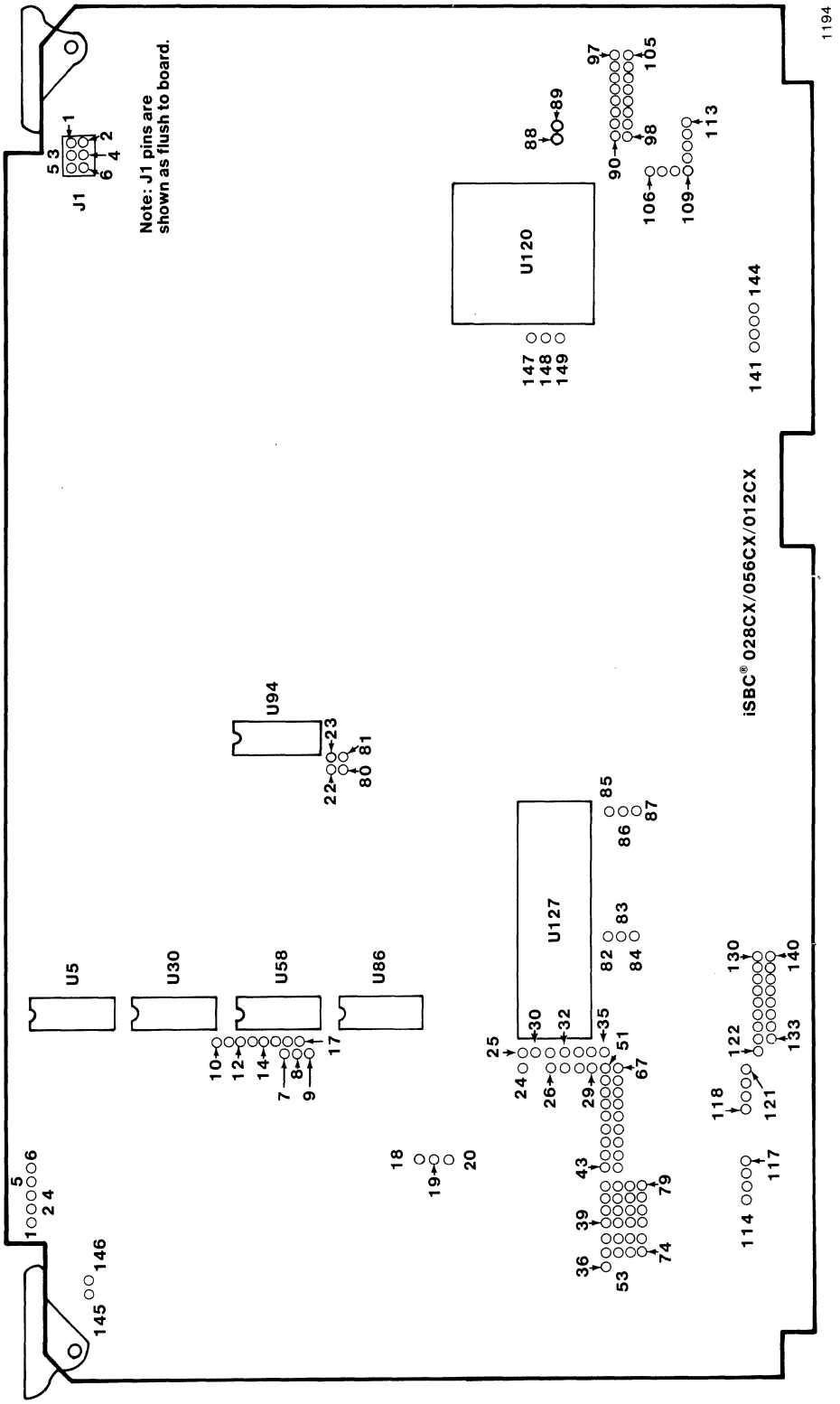

Figure 2-5. Jumper Post Location Diagram

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CHAPTER 3
ECC OPERATION AND PROGRAMMING INFORMATION

3.1 INTRODUCTION

The iSBC CX-Series RAM boards each use two special registers to pass ECC mode control and status information to and from the system master iSBC board. These registers are called the Control Status Register (CSR) and the Error Status Register (ESR). This chapter describes the two registers, and explains how to program them for the desired operations. Board initialization procedures are given in Section 3.5.

3.2 MODES OF ECC OPERATION

There are six ECC modes of operation on this series of RAM boards. Each mode is obtained by software programming from the master iSBC board. The six modes are:

a. Interrupt on any error mode;
b. Interrupt on non-correctable error only mode;
c. Correcting mode;
d. Non-correcting mode;
e. Diagnostic mode;
f. Examine syndrome word mode.

Modes (a) and (b) can be used in conjunction with modes (c) and (d). The modes are described in the following sections. Mode programming information is provided in Section 3.3.

3.2.1 INTERRUPT ON ANY ERROR MODE

In this mode the RAM board will interrupt the iSBC processor board when any error (single-bit or multiple-bit) is detected by the ECC circuitry. Interrupts are discussed in Section 2.4.5.

3.2.2 INTERRUPT ON NON-CORRECTABLE ERROR ONLY MODE

In this mode the RAM board will interrupt the iSBC processor board only when a non-correctable (multiple-bit) error is detected by the ECC circuitry. A multiple-bit error is not correctable by the ECC circuitry. Interrupts are discussed in Section 2.4.5.

3.2.3 CORRECTING MODE

In this mode the RAM board corrects any correctable error (single-bit error). Words which are not correctable are not modified. Interrupts are generated on any error only or on non-correctable errors only, depending on the mode selected. Interrupts are discussed in Section 2.4.5.

3.2.4 NON-CORRECTING MODE

In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described above. Interrupts are discussed in Section 2.4.5.

3.2.5 DIAGNOSTIC MODE

This mode is used for testing the on-board ECC circuitry. In this mode the Write Enable Strobe to the ECC RAM array is continuously disabled. The diagnostic mode can be used to simulate errors and in conjunction with the examine syndrome word mode to examine the check bits generated by the ECC circuitry. Refer to Section 4.3.3 for more Diagnostic Mode information.

3.2.6 EXAMINE SYNDROME WORD MODE

This mode, in conjunction with the diagnostic mode, is used for testing the ECC memory. In this mode, the syndrome bits (check bits) are clocked into the Error Status Register (ESR) on every memory read or write cycle. The ESR translation PROM (U155) switches to a transparent mode in the Examine Syndrome Word mode. This allows the actual syndrome word generated by the 82Ø6 device to be examined. The six ESR bits are gated onto MULTIBUS data lines DATØ/ - DAT5/. Refer to Section 4.3.3 for more Examine Syndrome Word Mode information.

3.3 PROGRAMMING INFORMATION

The following five sections describe how to program the Control Status Register (CSR) and how to read the Error Status Register (ESR). The CSR and the ESR provide a means of controlling and viewing the status of ECC operations. These registers are accessed via the system master iSBC board's I/O port addresses. The CSR is written to by asserting IOWC/ to the MULTIBUS lines and the ESR is read by asserting IORC/. Because the CSR and the ESR occupy the same I/O port, the CSR may not be read. The ESR is cleared by a write to the board I/O address.

CAUTION

The ECC circuitry could malfunction if the CSR is loaded at the same time an iLBX bus memory access is taking place. In a single CPU system, this means that there must be no DMA activity on the iLBX bus while the CPU is loading the CSR. In a multiple CPU system, ensure that one CPU is not loading the CSR while another CPU board is accessing the memory board via the iLBX bus.

3.3.1 CONTROL STATUS REGISTER (CSR) PROGRAMMING

The CSR is an eight-bit register (on the RAM board) which is programmed by the processor to select one of several operating modes. To program the CSR, assert IOWC/ when the port address and data are stable on the MULTIBUS lines. CSR format is shown below; a summary of programming is given in Table 3-1; Table 3-2 provides a list of the most typical ECC modes, shown in hexadecimal format. The codes shown can be written directly to the CSR, during system initialization. Table 3-1 also gives the condition of the CSR after a RESET or POWER-UP condition.

MSB LSB

B7	B6	B5	B4	B3	B2	B1	BØ

Table 3-1. RAM Board Control Status Register Format Summary

Bit Ø	Interrupt on Correctable Error: When this bit is low (Ø), a MULTIBUS interrupt is asserted only on an uncorrectable error. When this bit is high (1), the RAM board asserts a MULTIBUS interrupt on any data error (single or multiple-bit). POWER-UP & RESET CONDITION: HIGH (1)
Bit 1	Diagnostic Mode Select. When this bit is high (1), the diagnostic mode is deselected. When low (Ø), the diagnostic mode is selected. POWER-UP & RESET CONDITION: HIGH (1).
Bit 2	Correct/Non-Correcting Modes: When this bit is high (1) every correctable error which occurs will be corrected by the on-board circuitry. The RAM board will continue to overwrite even if an uncorrectable error occurs during write-byte cycles. An overwrite should be performed to clear errors during memory initialization. When this bit is low (Ø) the board will not correct any errors. The RAM board will abort write-byte cycles if an uncorrectable error is detected on the read portion of the cycle. Refer to Section 4.3 for additional information. POWER-UP & RESET CONDITION: HIGH (1)
Bit 3	Examine Syndrome Word Mode: When this bit is high (1), the Examine Syndrome Word mode is deselected. When this bit is low (Ø), the Examine Syndrome Word mode is selected. POWER-UP & RESET CONDITION: HIGH (1)
Bit 4	Reserved: must be low (Ø).
Bit 5	Reserved: must be low (Ø).
Bit 6	Reserved: must be low (Ø).
Bit 7	Reserved: must be low (Ø).

Table 3-2. Typical ECC Operating Modes (Hex)

Hex Code	Mode Description
ØF	Correcting, Interrupt on Correctable Error.
ØE	Correcting, Interrupt on Non-Correctable Error.
ØB	Non-correcting, Interrupt on Correctable Error.
ØA	Non-correcting, Interrupt on Non-Correctable Error.
ØØ	Diagnostic mode, syndrome read selected.

NOTE

Memory must be cleared after a RESET, and before starting system write or read operations. Refer to Section 3.5.

3.3.2 INTERRUPT ON ANY ERROR MODE PROGRAMMING

Bit Ø selects the interrupt mode. When bit Ø is high, the RAM board will issue an interrupt to the MULTIBUS when any error is detected.

3.3.3 INTERRUPT ON NON-CORRECTABLE ERROR ONLY MODE PROGRAMMING

Bit Ø selects the interrupt mode. When bit Ø is low, the RAM board will issue an interrupt to the MULTIBUS only when a non-correctable error is detected.

3.3.4 CORRECTING AND NON-CORRECTING MODE PROGRAMMING

Bit 2 selects the correcting mode when high, or the non-correcting mode when low.

3.3.5 DIAGNOSTIC MODE PROGRAMMING

Bit 1 deselects the diagnostic mode when high, or selects the diagnostic mode when low. This mode can be used for simulating errors in memory. The simulated errors should be detected by the ECC circuitry. In this mode the Write Enable strobe to the ECC RAM array is continuously inactive.

3.3.6 EXAMINE SYNDROME WORD MODE PROGRAMMING

Bit 3 deselects the examine syndrome word mode when high (1), or selects the examine syndrome word mode when low (Ø). The examine syndrome word mode is used in conjunction with the diagnostic mode. This mode allows testing the check bit generation circuitry of the board. In this mode, the syndrome (check) bits are clocked into the error status register upon every read (or write) cycle. Refer to Section 4.3 for additional information on this mode.

Table 3-3. RAM Board Error Status Register Format

Bit 6 5	Meaning
Ø Ø	Error in row Ø
Ø 1	1
1 Ø	2
1 1	3

Bit 4 3 2 1 Ø	Meaning
Ø Ø Ø Ø Ø	Error in data bit Ø
Ø Ø Ø Ø 1	1
Ø Ø Ø 1 Ø	2
Ø Ø Ø 1 1	3
Ø Ø 1 Ø Ø	4
Ø Ø 1 Ø 1	5
Ø Ø 1 1 Ø	6
Ø Ø 1 1 1	7
Ø 1 Ø Ø Ø	8
Ø 1 Ø Ø 1	9
Ø 1 Ø 1 Ø	1Ø
Ø 1 Ø 1 1	11
Ø 1 1 Ø Ø	12
Ø 1 1 Ø 1	13
Ø 1 1 1 Ø	14
Ø 1 1 1 1	15
1 Ø Ø Ø Ø	Error in check bit Ø
1 Ø Ø Ø 1	1
1 Ø Ø 1 Ø	2
1 Ø Ø 1 1	3
1 Ø 1 Ø Ø	4
1 Ø 1 Ø 1	5
1 1 1 1 Ø	No error.
1 1 1 1 1	Non-correctable (multiple-bit) error.

Note: Bit 7 is always high.

3.4 ERROR STATUS REGISTER (ESR)

This 7-bit register contains information about memory errors. The ESR reflects the latest error occurrence.

As shown in Table 3-3, bits 5 and 6 indicate the memory row number and bits Ø - 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome word) is in error. Bit 7 is always high.

3.5 SOFTWARE INITIALIZATION PROCEDURE

The following steps provide summarized programming information for the system initialization sequence.

Step 1: Power on.

Step 2: Reset.

Step 3: Disable interrupts on the processor.

Step 4: Set the CSR to "CORRECT" mode.

Step 5: Write Ø's to all memory locations.

Step 6: Set the CSR to the desired operating mode, as described in Tables 3-1 and 3-2.

Step 7: Enable interrupts on the processor.

***

CHAPTER 4
MEMORY BOARD OPERATION

4.1 INTRODUCTION

This chapter describes basic operations on the iSBC CX-Series RAM boards. The boards operate in an identical manner. The differences between the boards are memory capacity (see Chapter 1) and the deselect option (see Chapter 2). The boards can be accessed by both the MULTIBUS interface and the iLBX Bus interface.

4.2 MEMORY OPERATIONS

Data is transferred between the MULTIBUS interface or the iLBX bus and the on-board RAM chips via bidirectional data buffers that maintain signal compatibility between the board and the bus. ECC operations are discussed separately in Section 4.3.

The following discussion refers generally to both iLBX bus and MULTIBUS interface operations. Although the two buses do not operate in an identical fashion, the scope of this discussion allows merging the two into one section. For additional information on the MULTIBUS interface, refer to the INTEL MULTIBUS SPECIFICATION; for iLBX bus information, refer to the INTEL iLBX BUS SPECIFICATION.

A typical operation on the iSBC CX-Series RAM Boards is initiated when the bus master issues a memory address to all devices on the MULTIBUS interface. The address is decoded by the select logic on the RAM boards to prepare the boards for the command that is following. After sending the address, the bus master may issue the READ or WRITE command to start the operation. The command is placed onto the MULTIBUS interface a minimum of 5Ø nanoseconds after the address.

If a READ command is sensed (or $R/\overline{W}$ = 1 in iLBX bus operations) from the bus interface, the RAM boards perform a sequence of operations to READ data from the addressed memory location and place its contents onto the data lines (DATØ/ through DATF/). When the data has stabilized on the bus, the RAM boards issue a Transfer Acknowledge signal (XACK/ or ACK/ in iLBX bus operations) to the bus master indicating that the data is available. In response to the Transfer Acknowledge signal, the bus master accepts the data from the bus interface and removes the READ command (MRDC/) and the RAM address from the bus control and address lines.

If a WRITE command is sensed (or $R/\overline{W}$ = Ø in iLBX bus operations) from the bus interface, the RAM boards perform a sequence of operations to WRITE a data byte into the memory at the address provided by the bus master via the bus interface address lines (ADRØ/ through ADR17/). The bus master places the write data onto the bus interface coincident with issuing an address. The bus master then issues a WRITE command to the RAM boards after the data stabilizes on the bus interface.

On receiving the command, the RAM board performs the WRITE operation: a sequence of events to write the data byte from the bus interface into the addressed RAM memory location.

On completion of the WRITE operation, the control logic for the RAM boards send a Transfer Acknowledge signal (XACK/) to the bus master indicating that the operation is completed. In response to the XACK/ signal, the bus master removes the WRITE command (MWTC/) from the MULTIBUS interface. A minimum of 5Ø nanoseconds later, the bus master deactivates the data lines and the address lines on the MULTIBUS interface.

The refresh logic required by the dynamic RAM chips is on the board. The refresh logic is capable of providing refresh for one row of memory cells each 15 microseconds. An optional off-board RAM refresh request is sensed by the board logic when the REFRESH/ line on the P2 connector goes LOW. (The iLBX bus cannot be used if the external refresh is enabled by jumper connection. Refer to section 2.4 for jumper information.) After a refresh cycle is requested, the actual execution may be delayed, but never longer than one READ or WRITE cycle.

The iSBC Ø12CX/Ø1ØCX/Ø2ØCX boards also allow deselection of portions of their upper addressed memory. This allows the memory size of a board to appear smaller than it physically is. This option, however, forces the base address of the board to Ø. Deselection of the MULTIBUS and iLBX memories are handled differently; configuration data and jumper connections for both are covered in Section 2.4.1.5 and Tables 2-6 through 2-9.

4.3 ERROR CHECKING AND CORRECTION (ECC) OPERATION

The basic function of the on-board ECC circuitry is to detect any memory errors which occur during read operations. In the correcting mode, the board will then correct any single-bit errors. In the non-correcting mode, errors are still detected, but no action is taken to correct any bits. A correction cycle adds about 255 nanoseconds to the overall READ or WRITE cycle.

ECC operations are performed by an on-board Intel 82Ø6 Error Detection and Correction Unit (device U12Ø). The 82Ø6 unit uses a separate group of RAM devices for its own memory operations. The 82Ø6 unit uses a modified Hamming code to generate check bits for each 16-bit data word. Each data word has an associated 6-bit check bit word, stored in ECC memory.

When a particular data word is read, the ECC circuitry generates a new group of check bits and compares these to the check bits already stored in ECC memory. If the two check bit words are equal, no error has occurred. If the words do not match, an error has occurred.

From this point, several optional actions can take place. Assuming the board is in the correcting mode, and a single-bit (correctable) error occurs, the 82Ø6 unit will correct the data word to its original value.

The 82Ø6 correction unit creates an 7-bit syndrome word which contains the location of the error. The syndrome word is latched into the Error Status Register (ESR). The ESR can then be read by the host processor board, through the board I/O port, for error-logging purposes. Refer to Section 3.4 for more information about the ESR. If the interrupt mode has been enabled, a MULTIBUS interrupt will be generated.

When a multiple-bit error occurs, no correction action is possible. However, a syndrome word is generated for error logging purposes, and a MULTIBUS interrupt is always generated when a non-correctable error occurs.

In a full 16-bit word write operation, data is written directly to memory and to the 82Ø6 correction unit at the same time. The 82Ø6 correction unit generates the check bit word and places this into ECC memory.

For 8-bit byte write operations, part of the data word is overwritten and part is retained in memory. This is accomplished by performing a "write-byte" cycle. During this operation, the complete old word is read into the 82Ø6 correction unit and corrected, with the syndrome word internally latched. Only that part of the word not to be modified is output. The part of the word to be overwritten is supplied by the MULTIBUS or iLBX bus. The 82Ø6 correction unit then calculates check bits for the new word, using the byte from the previous read operation and the new byte from the system bus, and writes them into memory.

Board ECC operations are slightly different for MULTIBUS and iLBX bus operations. The following sections describe each bus ECC operation. During MULTIBUS read and write operations, all ECC activity is carried on in parallel with data transfers. However, in iLBX read operations, ECC activity is carried on in a serial fashion. A simplified block diagram illustrates this concept (see Figure 4-1). The following sections describe these operations in greater detail.

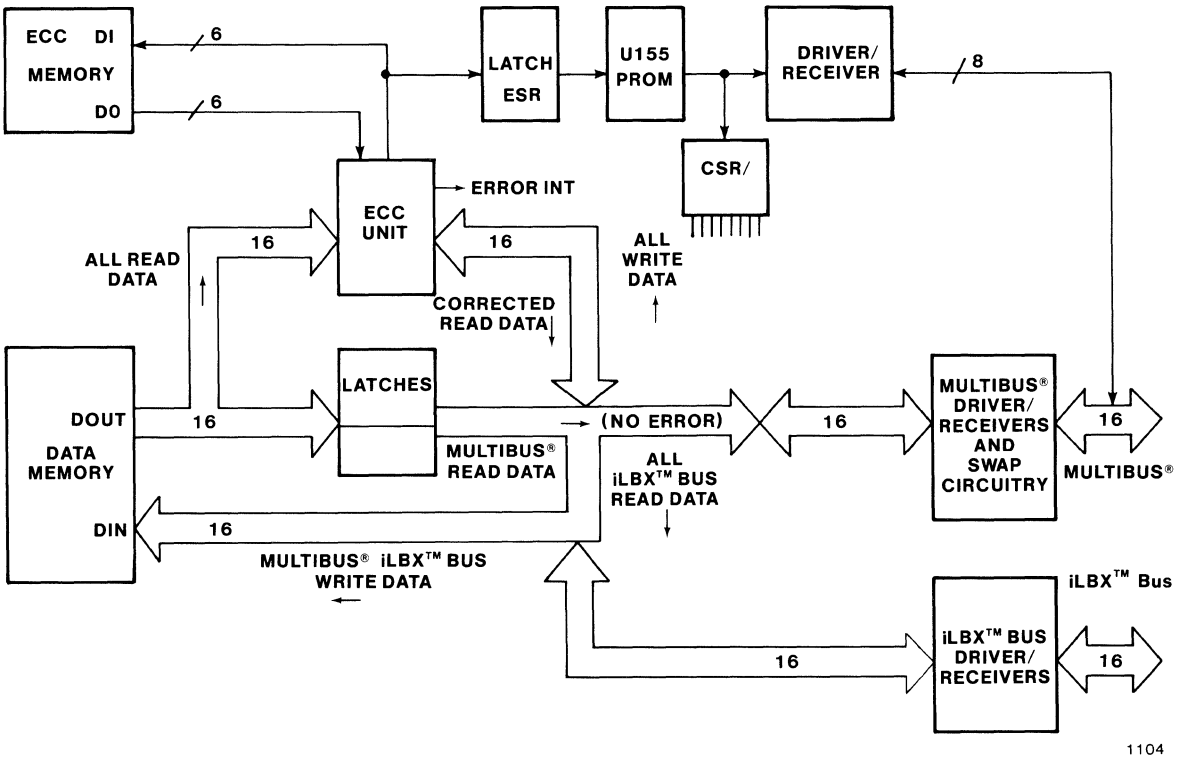


Figure 4-1. Data Path Simplified Diagram

4.3.1 MULTIBUS® ECC OPERATION

During a MULTIBUS write operation, the data word is written directly into memory. At the same time the data word is examined by the ECC circuitry to produce the corresponding check bit word. The check bit word is then stored in ECC memory. See Figure 4-1.

During a MULTIBUS read operation, the data word is latched in a register and released to the MULTIBUS buffers. While latched, the data word is also examined by the ECC circuitry. If the ECC check bit words are equal (indicating no error), the MULTIBUS XACK/ signal (Transaction Complete) is generated. If the check bit words do not compare (indicating an error), an error has occurred, and the board will respond as programmed previously by the Control Status Register. If the correcting mode was selected, and the error was a single-bit error, the corrected data word is gated from the ECC unit onto the MULTIBUS path (refer to Figure 4-1). Notice that the corrected word is not placed into memory. In addition, when an error (MULTIBUS interface only) is detected and corrected, the read-access and cycle times of the board are extended by a maximum of 255 nanoseconds. Refer to Section 4.3.

4.3.2 iLBX™ BUS ECC OPERATION

During an iLBX bus write operation, the data word is written directly into memory. At the same time, the data word is examined by the ECC circuitry to produce the corresponding check bit word. The check bit word is then stored in ECC memory. See Figure 4-1.

During an iLBX bus read operation, the data word is not latched in a register before release to the buffers. Instead, the data word is transferred directly into the 82Ø6 unit for ECC operations. This is done because of certain iLBX bus timing requirements. The timing of the iLBX bus is such that higher efficiency is obtained by allowing the data to be examined and/or corrected by the ECC circuitry in all read operations. This scheme permits the iLBX bus read to operate at top speed on every cycle, regardless of error detection.

4.3.3 DIAGNOSTIC MODE

When the board is in the diagnostic mode, it is possible to verify several ECC operations. Typically, there are three diagnostic operations which can be performed:

a. Examine the check bits generated during the write cycle.

b. Generate error, and examine the syndrome word generated during a read cycle.

c. Examine the check bits stored in ECC memory.

The first two options (a & b) are typically the most useful diagnostic operations. All three operations are described in the following paragraphs. Refer to Figure 4-1 for related information.

To verify that the on-board ECC circuitry is generating the appropriate check bits during a write cycle (option a above), program the CSR to the examine syndrome mode (refer to Tables 3-1 and 3-2 for programming information), write data to memory, and read the check bits in the ESR. Notice that the data in the CSR will be updated each cycle, since the latch that stores this data is clocked on each cycle. The check bits are routed through the syndrome word PROM encoder before reaching the ESR. However, this PROM is in the transparent mode while in the examine syndrome mode, thus allowing actual check bits to be examined.

To verify that the on-board ECC circuitry is generating the appropriate syndrome word during a read cycle (option b above), first write all zeros to memory. Next, enter the diagnostic mode, thus disabling any further changes to ECC memory, then change the data memory to any value other than zero, such as, write ØØØ1 to the data memory. Since you are in the diagnostic mode, no changes are made to ECC memory. Now, during a read cycle, each syndrome word will contain an error code. To verify the check bits stored in ECC memory, first write data to the memory. Next, enter the examine syndrome mode, and do an I/O READ from the ESR. The six low order bits of the ESR correspond to the check bits stored in ECC memory.

4.4 MULTIBUS® LOCK/ AND iLBX™ BUS LOCK/ SIGNALS

The iSBC CX-Series RAM boards can respond to two separate "LOCK" signals. The MULTIBUS LOCK/ signal enters the board at P1-25. The iLBX bus LOCK/ signal enters the board at P2-53. In each bus, the LOCK/ signal is asserted by a master CPU board to prevent another master from accessing the board through the other bus. For example, if master "A" is reading data from the board over the MULTIBUS lines and needs to keep master "B" from accessing the board over the iLBX bus, then master "A" must assert its MULTIBUS LOCK/ signal.

To lock the iLBX bus master off the RAM board, the MULTIBUS master board must assert its LOCK/ signal at least 15 nanoseconds prior to the rising edge of the current command (MRDC/ or MWTC/). The LOCK/ signal must be held active until 1ØØ nanoseconds after the falling edge of the command, of the last locked cycle. Similarly, to lock the MULTIBUS master off the RAM board, the iLBX bus master board must assert its LOCK/ signal at least 15 nanoseconds prior to the rising edge of the DSTB/ (Data Strobe) signal, and hold LOCK/ active until locked cycles are completed. In summary, when a CPU board asserts the LOCK/ signal, all "dual-ported" memory resources will be locked from access by another bus.

***

CHAPTER 5
SERVICE INFORMATION

5.1 INTRODUCTION

This chapter provides service assistance information, a RAM device location diagram, and schematic diagrams for the iSBC CX-Series RAM boards.

5.2 SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following telephone numbers for contacting the Intel Product Service Hotline:

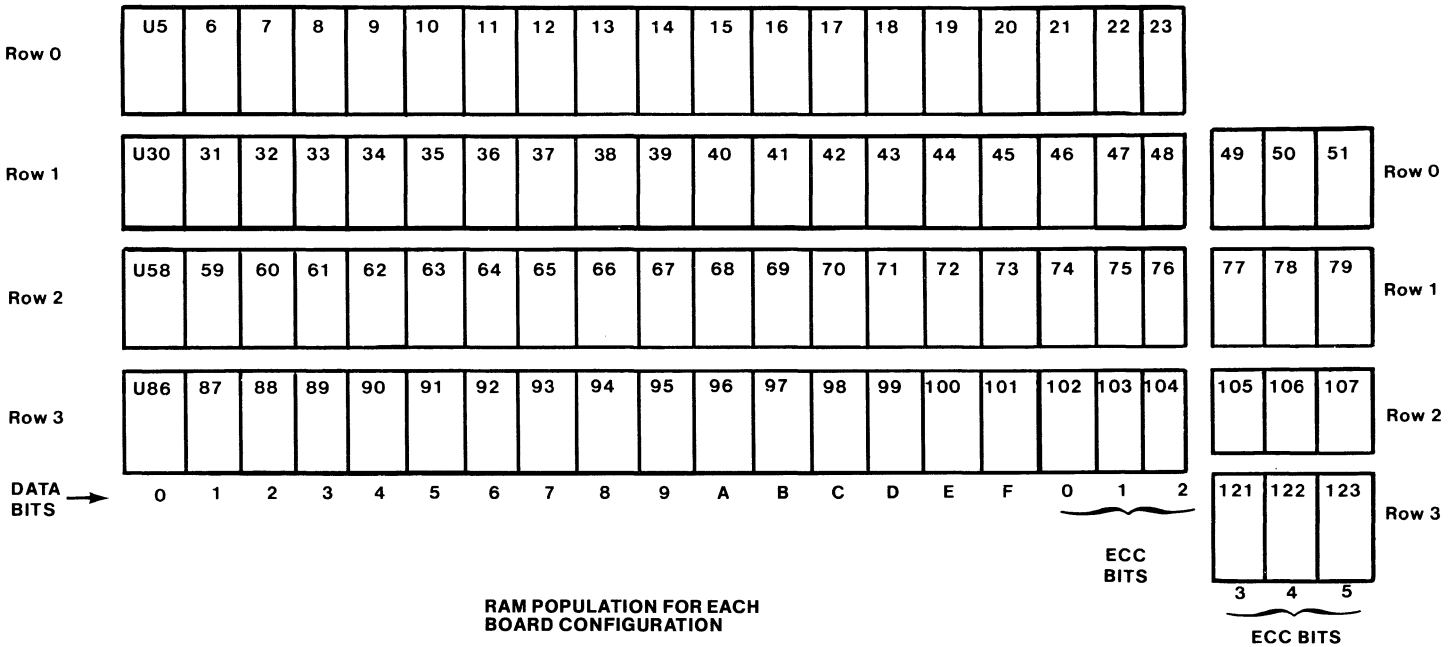
Western Region	(6Ø2) 869 - 4951
Midwestern Region	(6Ø2) 869 - 4392
Eastern Region	(6Ø2) 869 - 4Ø45
International	(6Ø2) 869 - 4862
TWX Number	91Ø - 951 - 133Ø

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 24Ø, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5.3 SCHEMATIC DIAGRAMS

Figure 5-1 shows the RAM device locations. Figure 5-2 (1Ø sheet set) shows the schematic diagrams for the iSBC Ø12CX RAM Board and are used to represent the iSBC Ø28CX/Ø56CX/Ø12CX/Ø1ØCX/Ø2ØCX RAM Boards. For current, individual board schematics, refer to the set of schematic diagrams shipped with each RAM board. The latest version of the schematic is shipped with each board. Keep these diagrams for future reference.

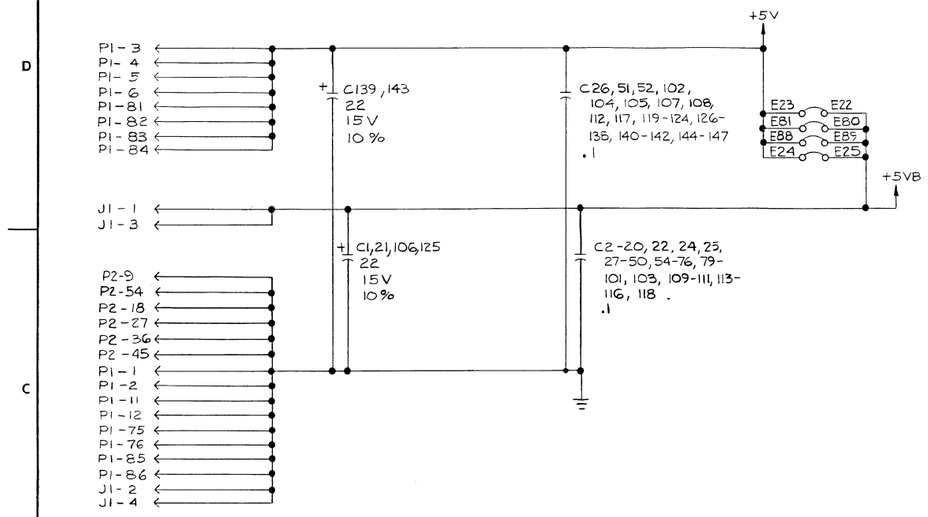


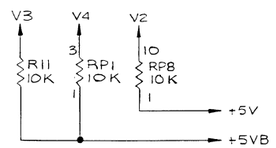
RAM POPULATION FOR EACH BOARD CONFIGURATION

iSBC® 028CX - DEVICES IN U5-23 AND 49-51
iSBC® 056CX - DEVICES IN U5-23, 30-51 AND 77-79
iSBC® 012CX - DEVICES IN U5-23, 30-51, 58-79, 86-107 AND 121-123
iSBC® 010CX - DEVICES IN U5-23, 30-51, AND 77-79
iSBC® 020CX- DEVICES IN U5-23, 30-51, 58-79, 86-107 AND 121-123

1105

Figure 5-1. iSBC® CX-Series Board RAM Device Location Diagram





DEVICE TABLE

REFERENCE DESIGNATION	DEVICE TYPE	POWER PINS GND	+5V	+5VB	UNUSED LOGIC ELEMENT OUTPUT PINS
U3,55	74S00	7		14	
U125,140	74S00	7	14		
U111,119,137	74S02	7	14		
U57,145,112	74S04	7		14	
U117	74S04	7	14		
U148	74S05	7	14		U148-10,12
U53	74S22	7	14		
U2	74S08	7		14	
U80,146	74S08	7	14		
U113	74S10	7		14	
U27	74S11	7		14	
U81,131	74S11	7	14		
U124	74S20	7	14		
U54	74S22	7		14	
U28,118	74S32	7	14		
U114	74S32	7		14	
U25	74S37	7	14		
J26	74S37	7		14	
U4	74S38	7		14	U4-3,6
U82	74S51	7		14	
U85	74S64	7		14	
U83,84	74S64	7	14		
U29,110,116,126,130	74S74	7	14		
U1	74S74	7		14	
U132, U138	74S112	8	16		
U56	74S132	7		14	
U133	74LS139	8	16		
U143	74S175	8	16		
U115	74S240	10		20	
U139,149	74S240	10	20		U159-9
U151,159,160					U151-9
U150,161,162	74LS240	10	20		
U156,165,166	74LS245	10	20		
U134	74S260	7	14		
U147	74LS273	10	20		
U141, 142	74S283	8	16		
U144,153	74LS373	10	20		
U154,163,164	74LS640	10	20		
U157,167,168	74S373	10	20		
U136	74S374	10	20		U136-2,5,9,12,15,16
U5-23,30-51					
U58-79,86-107	2164	16		8	
U121,122,123					
U127	2964B	30		10	
U120	8206	26,43	60		
[3] U128,129,152,158	PAL16L8	10	20		
[3] U155	7649-5	10	20		
U52	DDU 100	7	14		
U108	DDU 250	7		14	
U24	DDU 300	7		14	
[3] U135	PAL16R4	10	20		
U109	DDU 100	7		14	

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE
A	ECO 40-4222	D.N.	2-13-84	[illegible]	2/17/84	[illegible]	3/14/84

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V, +80%,-20%.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, ±5%.
[3] THESE PARTS ARE PROGRAMMED.
[4] R3 IS NOT INSTALLED.
[5] JUMPER FROM E90 TO E98.
IN: DISABLE LBX
OUT: ENABLE LBX

UNUSED RP RESISTORS
RP3-7,8
RP7-9,10
RP2-4
RP10-5
RP1-7,8

REF DESIGNATION LAST USED	NOT USED
C149	E3,21,131,
DS1	E132,52
E149	
G1	
P2	
R20	
RP12	
U168	
J1	

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

ITEM NO	DESCRIPTION
	PARTS LIST

SIGNATURE	DATE
DRN BY [illegible]	2/3/84
CHK BY [illegible]	
ENGR APVD A. Jones	3/14/84
APVD	
APVD	

intel® 3065 BOWERS AVE SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC iSBC 012CX

SIZE	DOC C	CL CODE	RLSE LVL	DOCUMENT NUMBER	REV
D	40	0100		146660	A

SCALE —— SHEET 1 OF 10

109515

Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 1 of 1Ø)

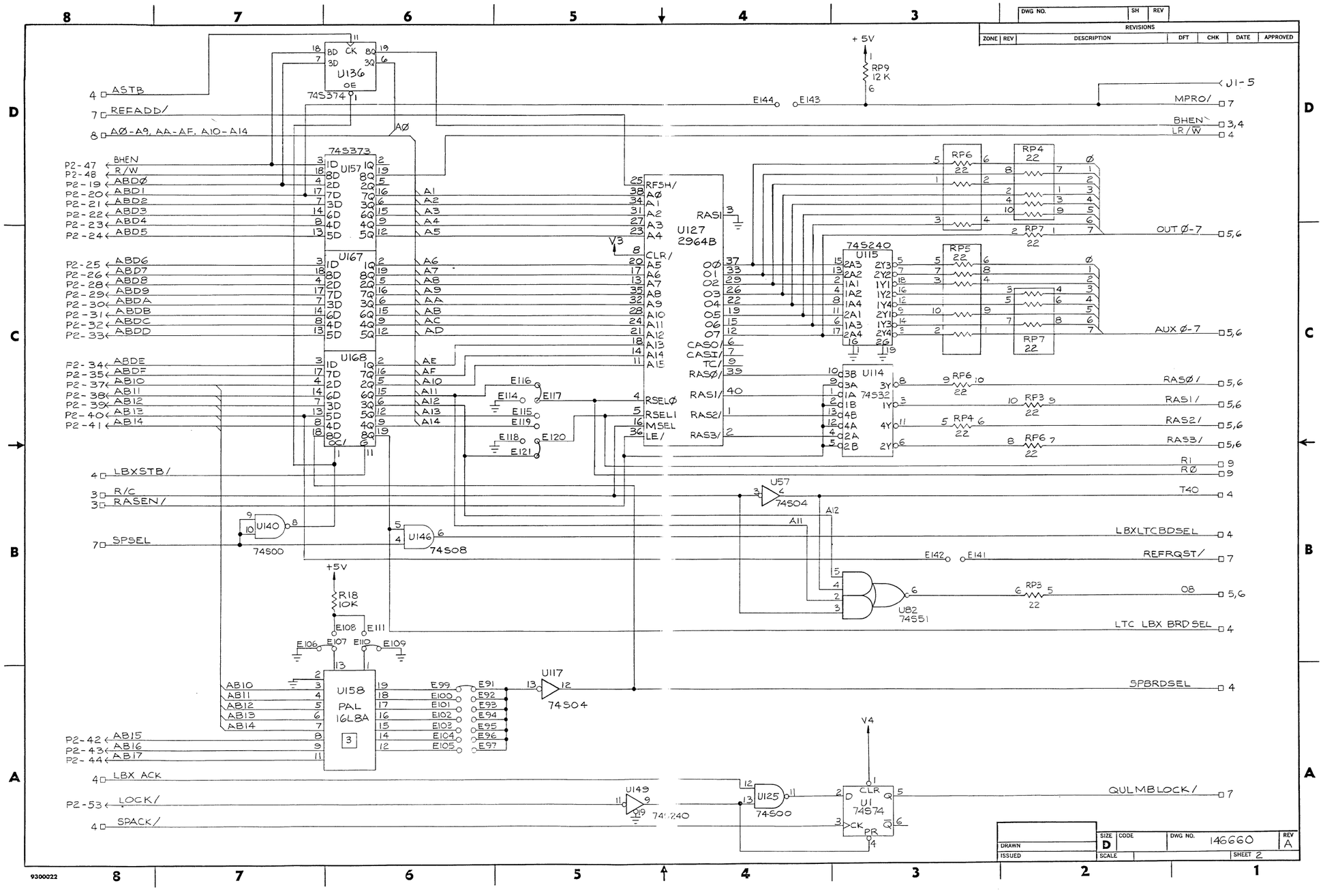


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 2 of 1Ø)

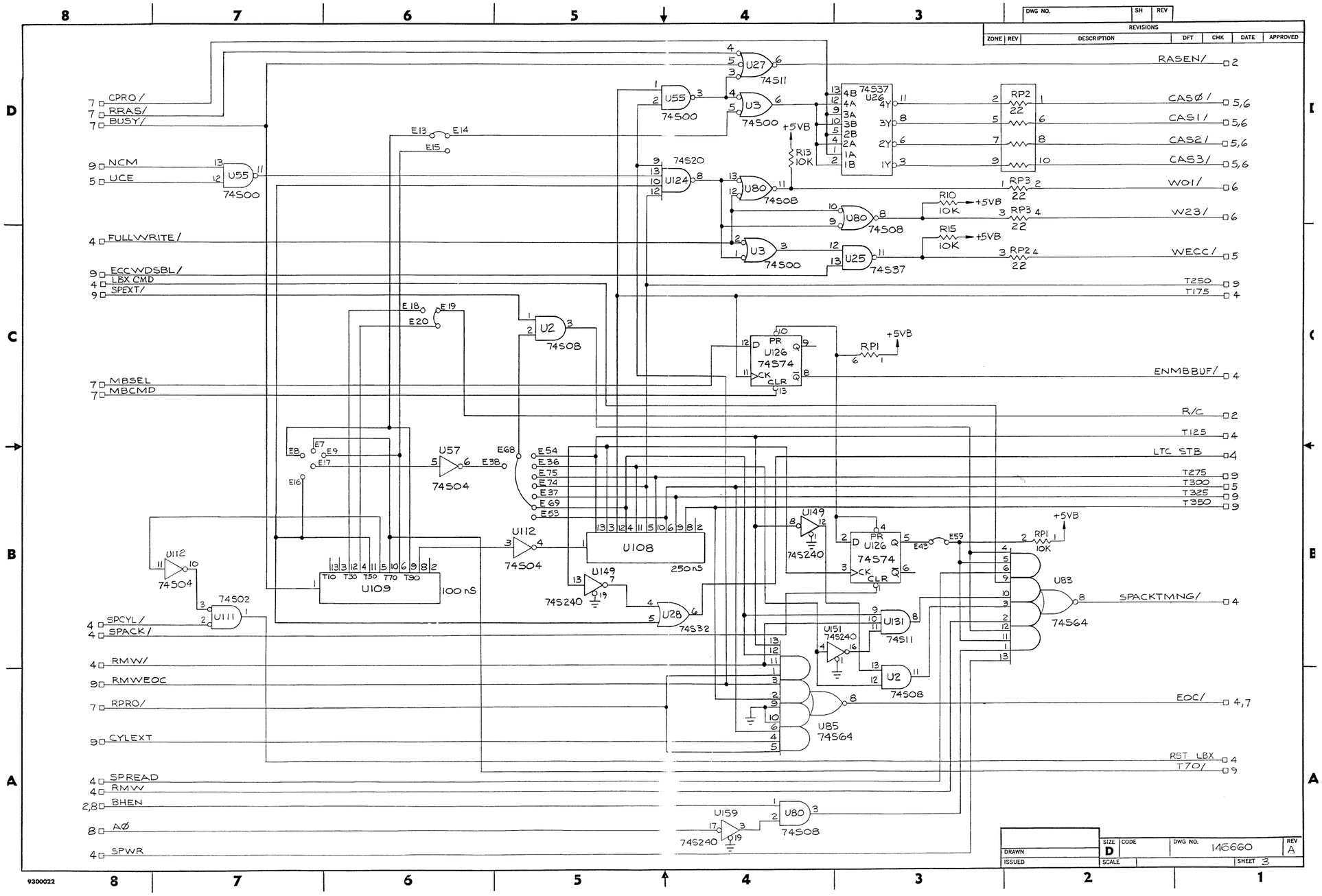


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 3 of 1Ø)

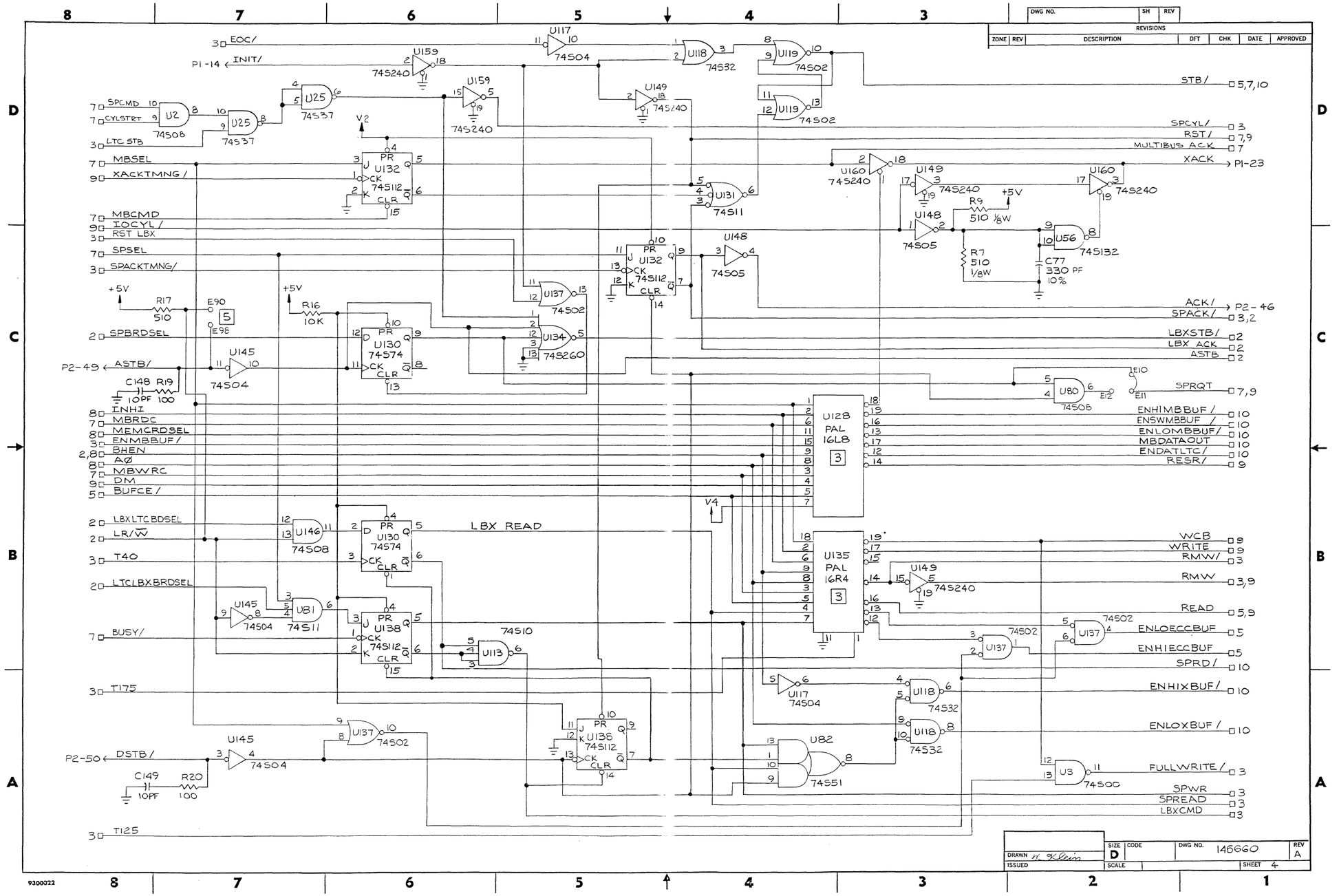


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 4 of 1Ø)

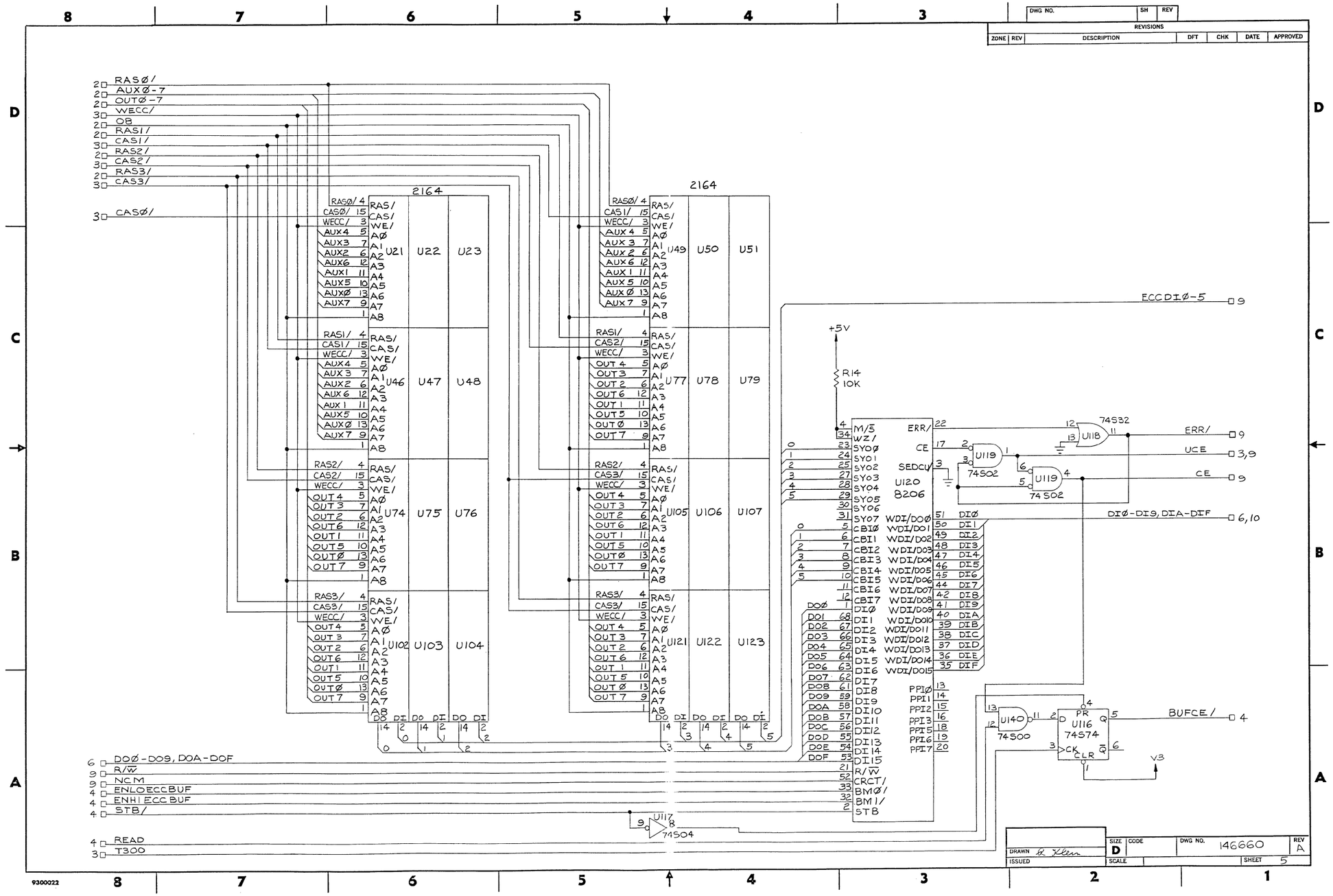


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 5 of 1Ø)

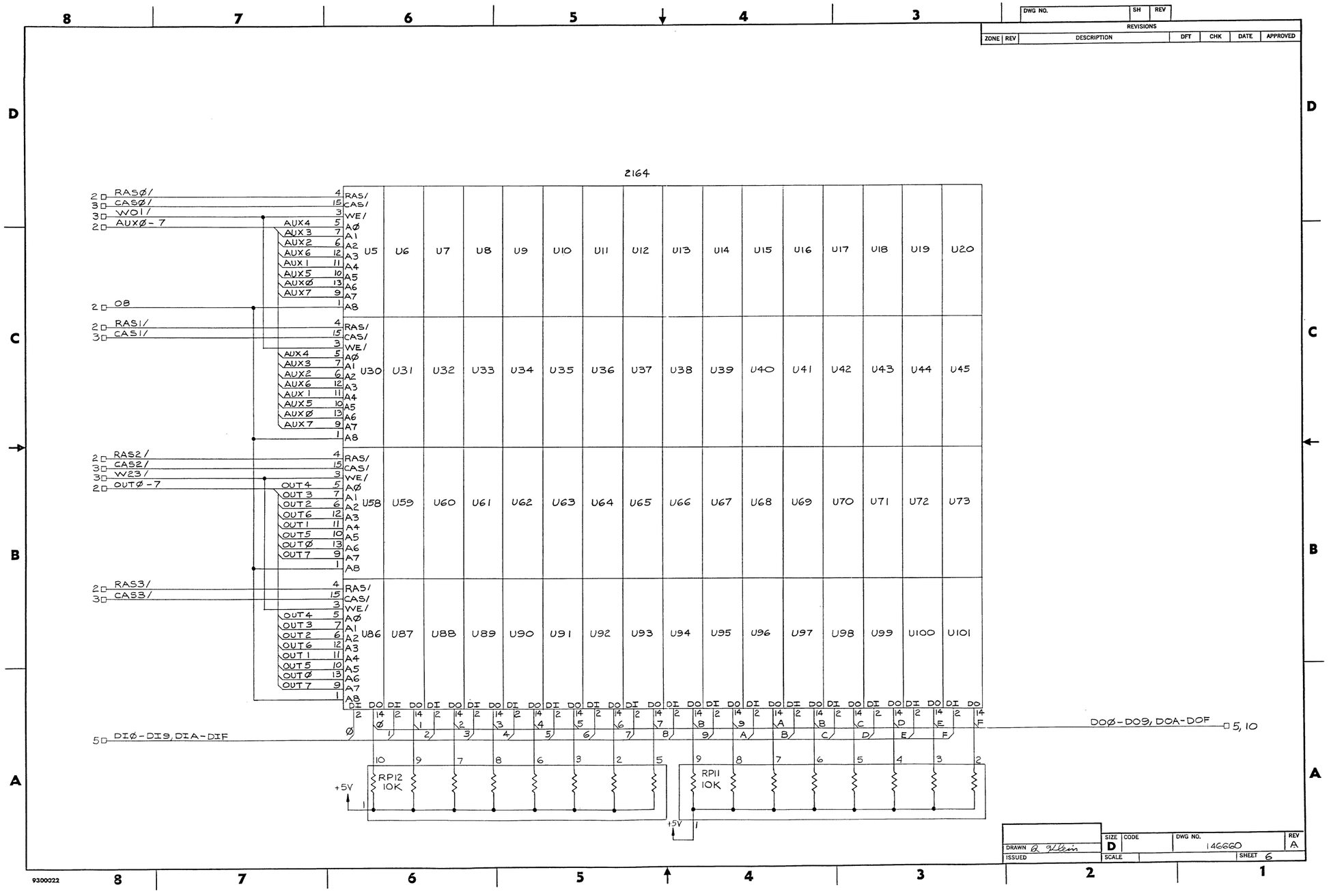


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 6 of 1Ø)

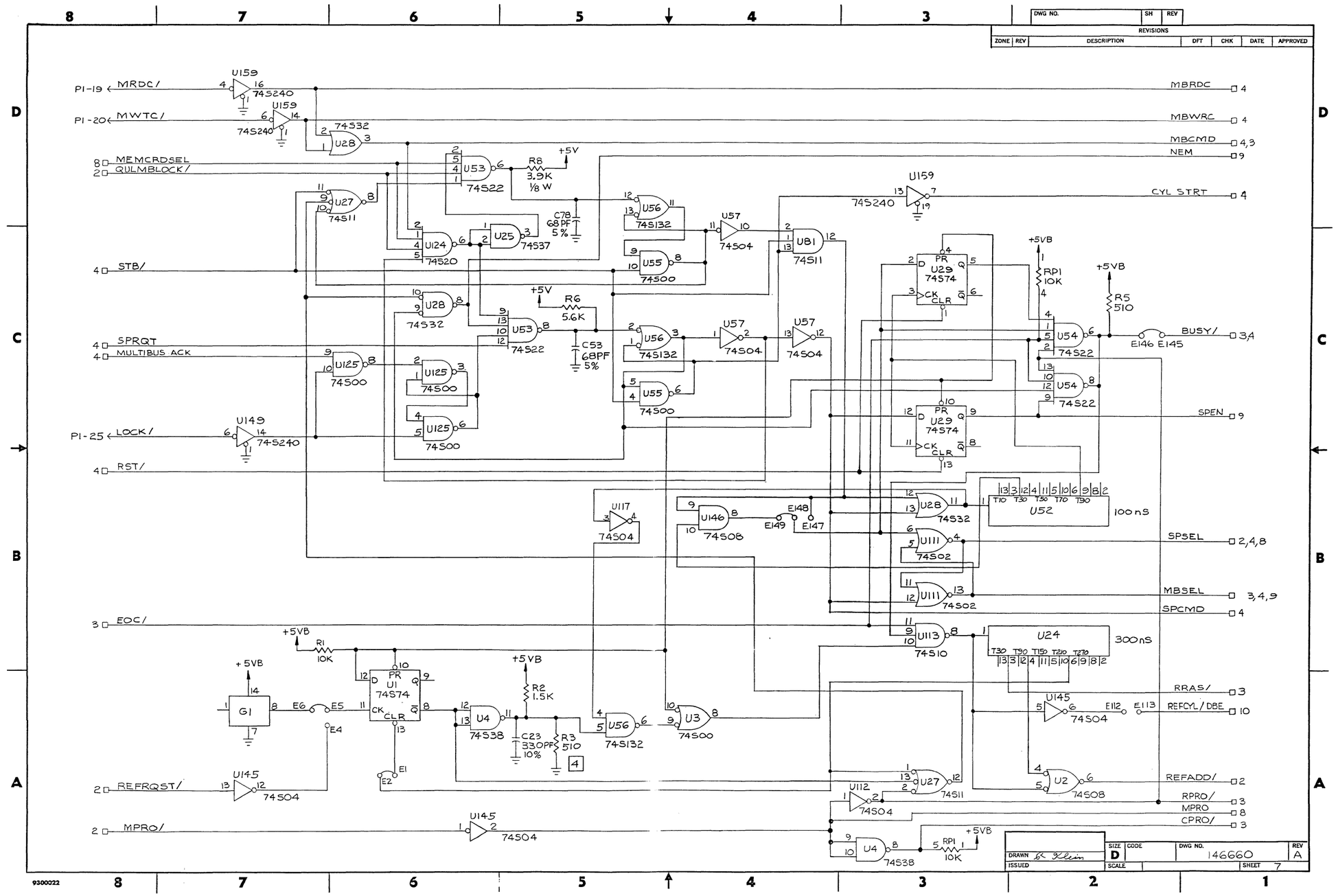


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 7 of 1Ø)

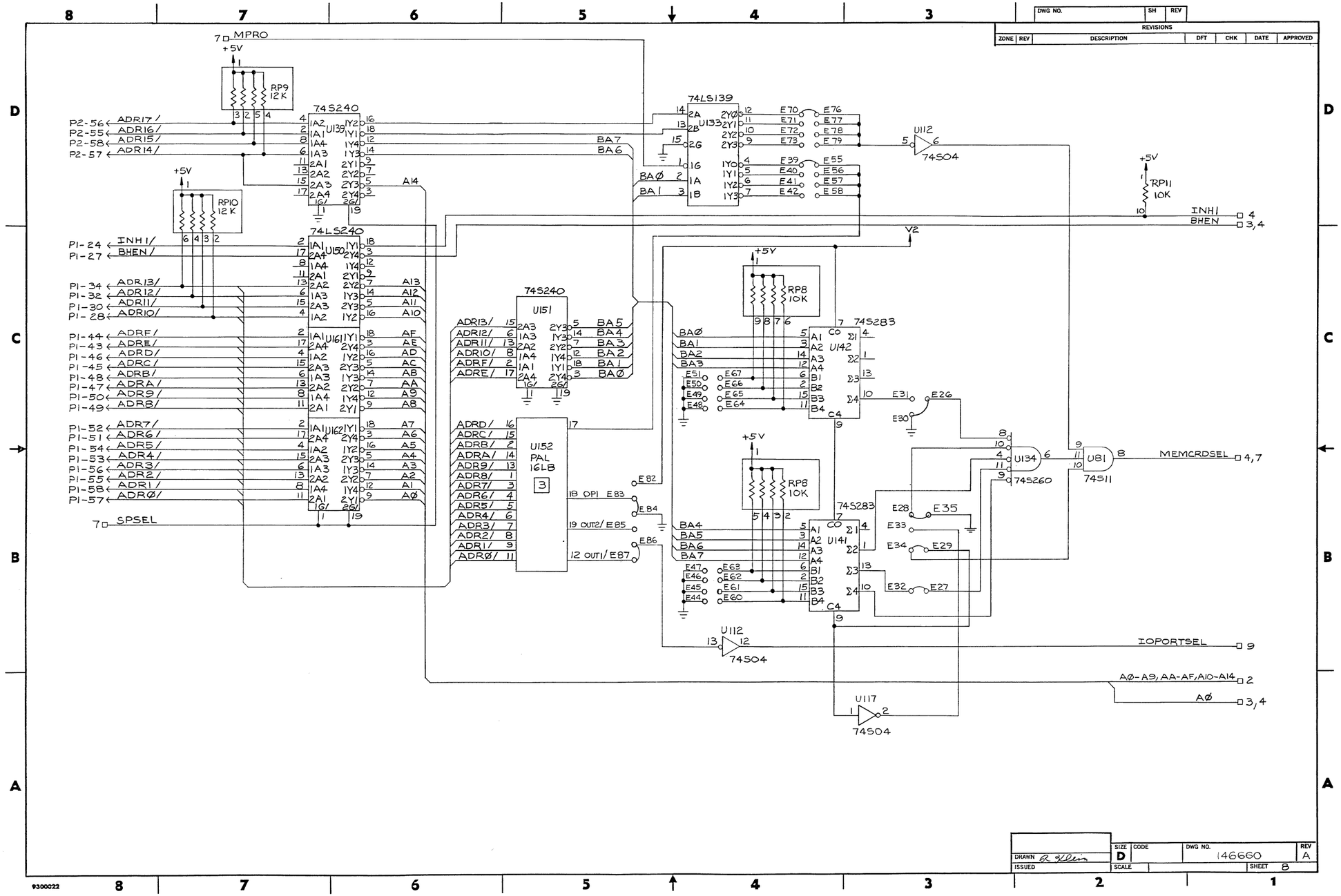


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 8 of 1Ø)

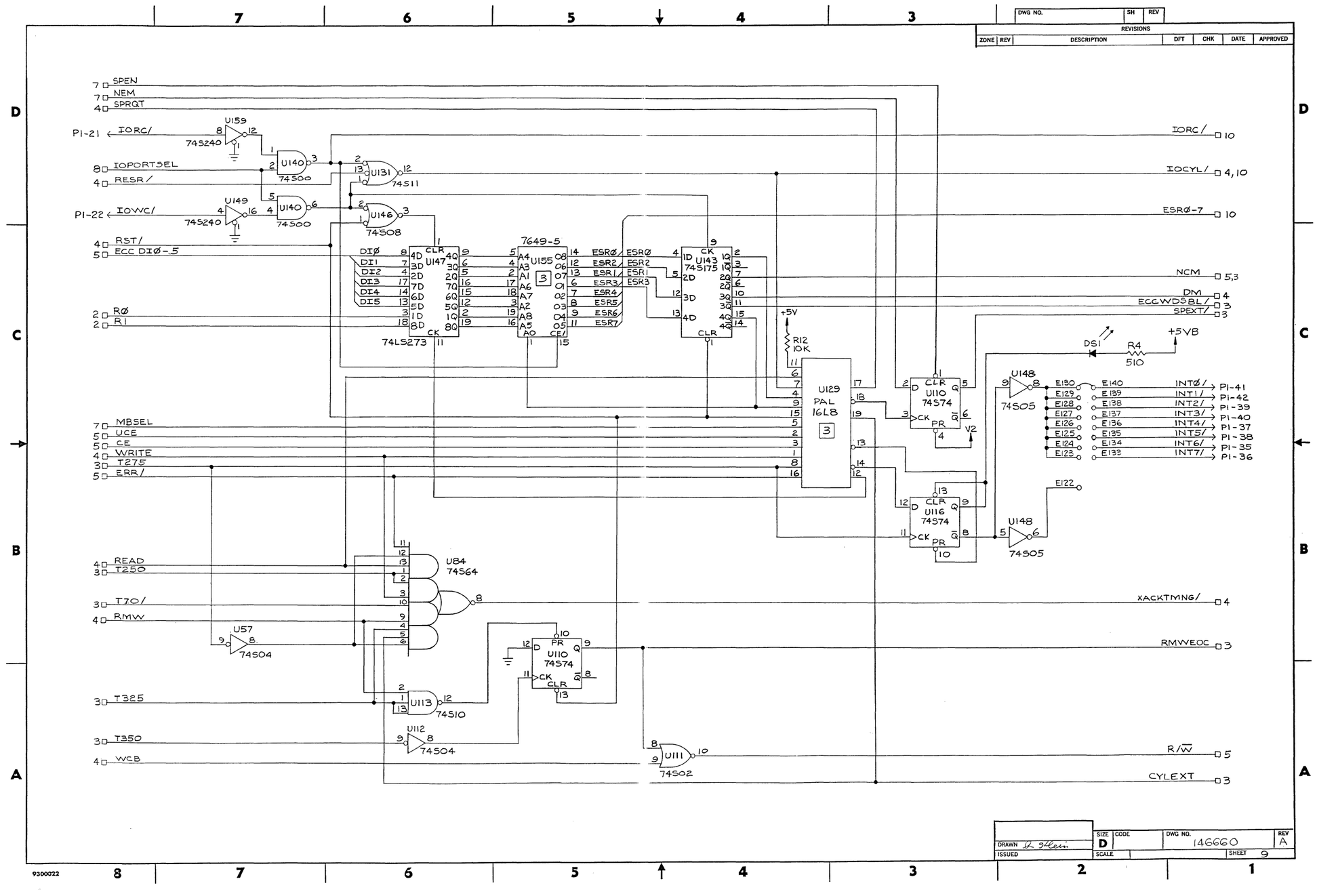


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 9 of 1Ø)

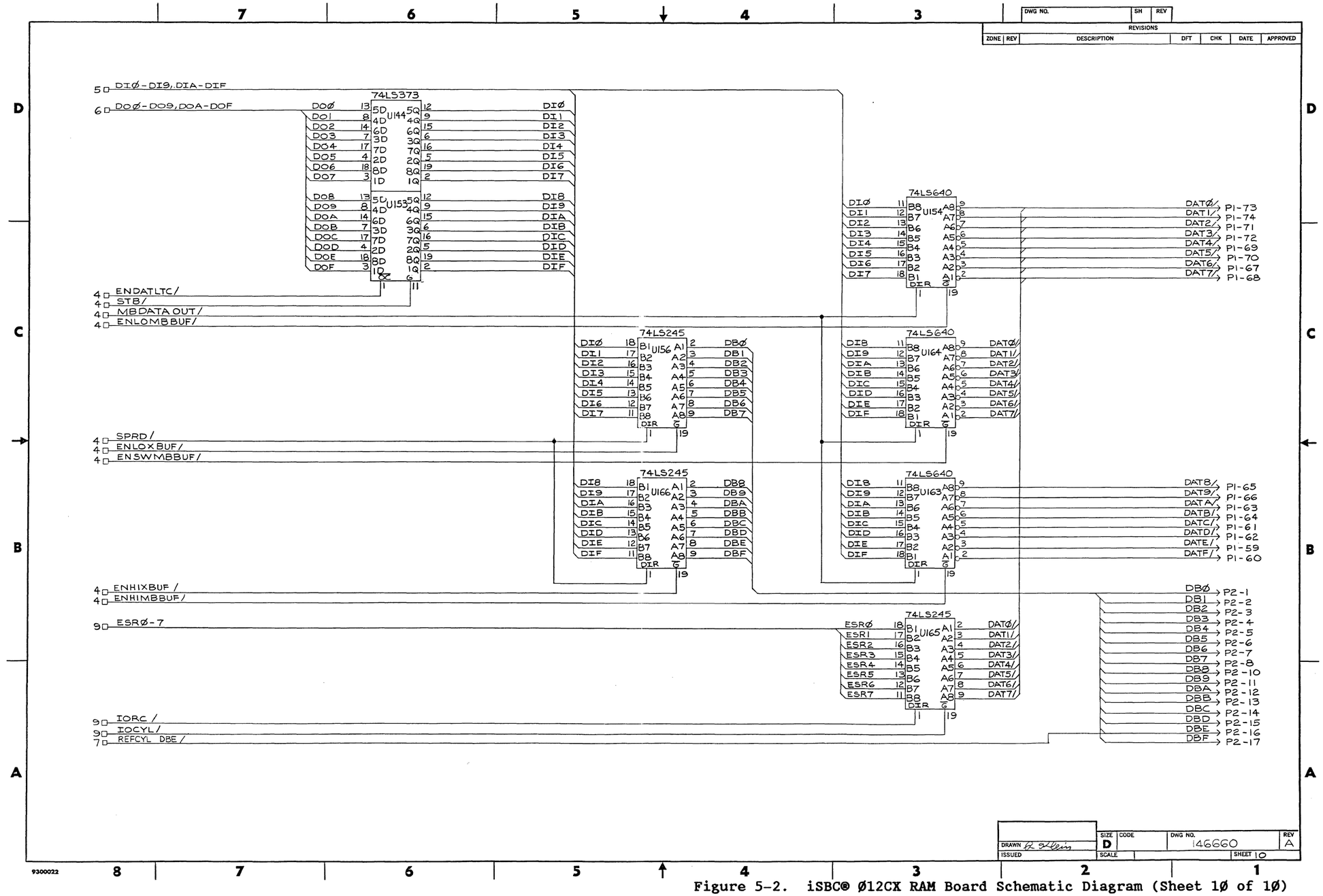


Figure 5-2. iSBC® Ø12CX RAM Board Schematic Diagram (Sheet 1Ø of 1Ø)

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APPENDIX A
CONNECTOR PIN ASSIGNMENTS

MULTIBUS connector P1 pin assignments are listed in Table A-1. The iLBX bus pin assignments for connector P2 and J1 are listed in Table A-2 and Table A-3 respectively.

Signal names indicate the active state of the signal on the MULTIBUS interface. If the signal name ends with a slash (/), the signal is active when LOW; if the signal does not end with a slash, the signal is active when HIGH.

Table A-1. MULTIBUS® Connector P1 Pin Assignments for iSBC® CX-Series RAM Boards

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5Vdc
	5	+5V	+5Vdc	6	+5V	+5Vdc
	7		Reserved	8		Reserved
	9		Reserved	1Ø		Reserved
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13		Reserved	14	INIT/	Reset
	15		Reserved	16		Reserved
	17		Reserved	18		Reserved
	19	MRDC/	Mem Read Cmd	2Ø	MWTC/	Mem Write Cmd
	21	IORC/	I/O Read Cmd	22	IOWC/	I/O Write Cmd
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
Bus Controls And Address	25	LOCK/	Lock	26		Reserved
	27	BHEN/	Byte High Enable	28	AD1Ø/	
	29		Reserved	3Ø	AD11/	Address
	31		Reserved	32	AD12/	Bus
	33		Reserved	34	AD13/	

Table A-1. MULTIBUS® Connector P1 Pin Assignments for iSBC® CX-Series RAM Boards (continued)

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Interrupts	35 37 39 41	INT6/ INT4/ INT2/ INTØ/	Parallel Interrupt Requests	36 38 4Ø 42	INT7/ INT5/ INT3/ INT1/	Parallel Interrupt Requests
Address	43 45 47 49 51 53 55 57	ADRE/ ADRC/ ADRA/ ADR8/ ADR6/ ADR4/ ADR2/ ADRØ/	Address Bus	44 46 48 5Ø 52 54 56 58	ADRF/ ADRD/ ADRB/ ADR9/ ADR7/ ADR5/ ADR3/ ADR1/	Address Bus
Data	59 61 63 65 67 69 71 73	DATE/ DATC/ DATA/ DAT8/ DAT6/ DAT4/ DAT2/ DATØ/	Data Bus	6Ø 62 64 66 68 7Ø 72 74	DATF/ DATD/ DATB/ DAT9/ DAT7/ DAT5/ DAT3/ DAT1/	Data Bus
Power Supplies	75 77 79 81 83 85	GND +5V +5V GND	Signal GND Reserved Reserved +5Vdc +5Vdc Signal GND	76 78 8Ø 82 84 86	GND +5 +5V GND	Signal GND Reserved Reserved +5Vdc +5Vdc Signal GND

Table A-2. iLBX™ Bus Connector P2 Pin Assignments for iSBC® CX-Series RAM Boards

Component Side			Solder Side		
Pin	Mnemonic	Signal Name	Pin	Mnemonic	Signal Name
1	DBØ	DATA LINE Ø	2	DB1	DATA LINE 1
3	DB2	DATA LINE 2	4	DB3	DATA LINE 3
5	DB4	DATA LINE 4	6	DB5	DATA LINE 5
7	DB6	DATA LINE 6	8	DB7	DATA LINE 7
9	GND	GROUND	1Ø	DB8	DATA LINE 8
11	DB9	DATA LINE 9	12	DB1Ø	DATA LINE 1Ø
13	DB11	DATA LINE 11	14	DB12	DATA LINE 12
15	DB13	DATA LINE 13	16	DB14	DATA LINE 14
17	DB15	DATA LINE 15	18	GND	GROUND
19	ABDØ	ADDRESS/DATA LINE Ø	2Ø	ABD1	ADDRESS/DATA LINE 1
21	ABD2	ADDRESS/DATA LINE 2	22	ABD3	ADDRESS/DATA LINE 3
23	ABD4	ADDRESS/DATA LINE 4	24	ABD5	ADDRESS/DATA LINE 5
25	ABD6	ADDRESS/DATA LINE 6	26	ABD7	ADDRESS/DATA LINE 7
27	GND	GROUND	28	ABD8	ADDRESS/DATA LINE 8
29	ABD9	ADDRESS/DATA LINE 9	3Ø	ABD1Ø	ADDRESS/DATA LINE 1Ø
31	ABD11	ADDRESS/DATA LINE 11	32	ABD12	ADDRESS/DATA LINE 12
33	ABD13	ADDRESS/DATA LINE 13	34	ABD14	ADDRESS/DATA LINE 14
35	ABD15	ADDRESS/DATA LINE 15	36	GND	GROUND
37	AB16	ADDRESS EXT. LINE 16	38	AB17	ADDRESS EXT. LINE 17
39	AB18	ADDRESS EXT. LINE 18	4Ø	AB19	ADDRESS EXT. LINE 19
41	AB2Ø	ADDRESS EXT. LINE 2Ø	42	AB21	ADDRESS EXT. LINE 21
43	AB22	ADDRESS EXT. LINE 22	44	AB23	ADDRESS EXT. LINE 23
45	GND	GROUND	46	ACK/	SLAVE ACKNOWLEDGE
47	BHEN	BYTE HIGH ENABLE	48	R/W	READ NOT WRITE
49	ASTB/	ADDRESS STROBE	5Ø	DSTB/	DATA STROBE
51	SMRQ/	Not Used On RAM Board	52	SMACK/	Not Used On RAM Bd.
53	LOCK/	ACCESS LOCK	54	GND	GROUND
55	ADR22/	MULTIBUS ADDRESS EXTENSION LINE 22	56	ADR23/	MULTIBUS ADDRESS EXTENSION LINE 23
57	ADR2Ø/	MULTIBUS ADDRESS EXTENSION LINE 2Ø	58	ADR21/	MULTIBUS ADDRESS EXTENSION LINE 21
59	RES	RESERVED	6Ø	TPAR/	TRANSFER PARITY

Table A-3. iLBX™ Bus Connector J1 Pin Assignments for iSBC® CX-Series RAM Boards

Pin	Signal Name
J1-1	+5V Battery In
J1-2	Ground
J1-3	+5V Battery In
J1-4	Ground
J1-5	Memory Protect (MPRO/)
J1-6	Reserved

***

APPENDIX B
PAL PROGRAMMING

B.1 INTRODUCTION

The iSBC CX-Series RAM boards utilize several pre-programmed PAL devices for configuration selection purposes. Although these devices cover a wide range of options, they may not include the desired configuration for your application. These pre-programmed devices may be removed and replaced with your own customized devices, to provide the desired configuration. This appendix provides guidelines for programming the two user-alterable PAL devices.

B.2 iLBX™ BASE ADDRESS PAL (U158)

This PAL is used to read the iLBX address lines and determine if the address on the lines is an on-board address. iLBX address lines AB1Ø through AB17 are connected directly to PAL inputs 3 through 11 (see Figure 5-2, sheet 2, and Section 2.4.1.4 of the text). Inputs 1 and 13 are used to select a range of addresses, and outputs 12, 14 through 19 select the specific group of 7 base addresses. Tables B-1 through B-5 show the specific programming used on the default part, for each board. The PAL is programmed differently for each version of the board.

B.3 ECC CONTROL PORT ADDRESS PAL (U152)

This PAL is used to read MULTIBUS address lines ADRØ/ through ADRD/. In conjunction with other circuitry, the PAL decodes the address used for I/O control and status information (for ECC). Two other inputs (17 & 18) to the PAL select specific groups of addresses (refer to Figure 5-2, sheet 8, and Section 2.4.2 in the text). Table B-6 shows the current programming used on the default part.

Table B-1. U158 PAL Programming for iSBC® Ø28CX Board

```
EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) /OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*/A20*A19*A18*A17
                EB*/EA*/IM*/A23*/A22*/A21*A20*A19*A18*/A17
IF (VCC) /OP1 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*/A18*/A17
                EB*/EA*/IM*/A23*/A22*/A21*A20*A19*A18*A17
IF (VCC) /OP2 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*/A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*/A17
IF (VCC) /OP3 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*A18*/A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*A17
IF (VCC) /OP4 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*/A19*A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*A18*/A17
IF (VCC) /OP5 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*/A18*/A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*/A19*A18*A17
IF (VCC) /OP6 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*A18*/A17
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*/A18*A17
                EB*/EA*/IM*/A23*/A22*A21*/A20*A19*/A18*/A17
DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC028C
 ACCORDING TO THE FOLLOWING TABLE:
EB    EA      OP #     STARTING ADDRESS

0     0       0         0K     (000000H)
0     0       1         128K   (020000H)
0     0       2         256K   (040000H)
0     0       3         384K   (060000H)
0     0       4         512K   (080000H)
0     0       5         640K   (0A0000H)
0     0       6         768K   (0C0000H)
0     1       0         896K   (0E0000H)
0     1       1         1024K  (100000H)
0     1       2         1152K  (120000H)
0     1       3         1280K  (140000H)
0     1       4         1408K  (160000H)
0     1       5         1536K  (180000H)
0     1       6         1664K  (1A0000H)
1     0       0         1792K  (1C0000H)
1     0       1         1820K  (1E0000H)
1     0       2         1948K  (200000H)
1     0       3         2076K  (220000H)
1     0       4         2204K  (240000H)
1     0       5         2332K  (260000H)
1     0       6         2560K  (280000H)
```

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F Ø F Ø F F F F 5 A F F 3 C F F F Ø F F F Ø F F F Ø F Ø F Ø F Ø .
F Ø Ø F F F F F A 5 F F 6 9 F F E 1 F F 1 E F F F Ø F Ø F Ø F Ø .
F Ø F Ø F F F F 5 A F F C 3 F F C 3 F F C 3 F F 3 C Ø F F Ø F Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B Ø B Ø B B B B 9 2 B B 3 8 B B Ø B B B B Ø B B B Ø B Ø B Ø B Ø .
B Ø Ø B B B B B 2 9 B B A 1 B B 1 A B B Ø B B B B Ø B Ø B Ø B Ø .
B Ø B Ø B B B B 9 2 B B 8 3 B B 3 8 B B B Ø B B Ø B Ø B B Ø B Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
```

Table B-2. U158 PAL Programming for iSBC® Ø56CX Board

```
EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) /OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18
                /EB*EA*/IM*/A23*/A22*/A21*A20*A19*A18
                EB*/EA*/IM*/A23*/A22*A21*A20*A19*/A18
IF (VCC) /OP1 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19*A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*/A19*/A18
                EB*/EA*/IM*/A23*/A22*A21*A20*A19*A18
IF (VCC) /OP2 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*/A19*A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*/A19*/A18
IF (VCC) /OP3 = /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19*A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*A19*/A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*/A19*A18
IF (VCC) /OP4 = /EB*/EA*/IM*/A23*/A22*/A21*A20*/A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*/A20*A19*A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*A19*/A18
IF (VCC) /OP5 = /EB*/EA*/IM*/A23*/A22*/A21*A20*/A19*A18
                /EB*EA*/IM*/A23*/A22*A21*A20*/A19*/A18
                EB*/EA*/IM*/A23*A22*/A21*/A20*A19*A18
IF (VCC) /OP6 = /EB*/EA*/IM*/A23*/A22*/A21*A20*A19*/A18
                /EB*EA*/IM*/A23*/A22*A21*A20*/A19*A18
                EB*/EA*/IM*/A23*A22*/A21*A20*/A19*/A18
```

DESCRIPTION:
THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC056C
ACCORDING TO THE FOLLOWING TABLE:

EB	EA	OP #	STARTING ADDRESS	
0	0	0	0K	(000000H)
0	0	1	256K	(040000H)
0	0	2	512K	(080000H)
0	0	3	768K	(0C0000H)
0	0	4	1024K	(100000H)
0	0	5	1280K	(140000H)
0	0	6	1536K	(180000H)
0	1	0	1792K	(1C0000H)
0	1	1	1948K	(200000H)
0	1	2	2204K	(240000H)
0	1	3	2460K	(280000H)
0	1	4	2716K	(2C0000H)
0	1	5	2972K	(300000H)
0	1	6	3228K	(340000H)
1	0	0	3484K	(380000H)
1	0	1	3740K	(3C0000H)
1	0	2	3996K	(400000H)
1	0	3	4252K	(440000H)
1	0	4	4508K	(480000H)
1	0	5	4764K	(4C0000H)
1	0	6	5020K	(500000H)

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F Ø F Ø F F F F F F F F 5 A F F 3 C F F F Ø F F F Ø F Ø F Ø F Ø .
F Ø Ø F F F F F F F F F A 5 F F 6 9 F F E 1 F F 1 E F Ø F Ø F Ø .
F Ø F Ø F F F F F F F F 5 A F F C 3 F F C 3 F F C 3 Ø F 3 C F Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B Ø B Ø B B B B B B B B 9 2 B B 3 8 B B Ø B B B B Ø B Ø B Ø B Ø .
B Ø Ø B B B B B B B B B 2 9 B B A 1 B B 1 A B B Ø B B Ø B Ø B Ø .
B Ø B Ø B B B B B B B B 9 2 B B 8 3 B B 3 8 B B B Ø Ø B Ø B B Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø .
```

Table B-3. U158 PAL Programming for iSBC® Ø12CX Board

```
PAL16L8                                                PAL DESIGN SPECIFICATION
DESELDEC                                               6/17/82  REVISED 12/1/83
LBX BUS ADDRESS DECODER   (512K) WITH DESELECT

EA  IM  A16  A17  A18  A19  A20  A21  A22  GND  A23  OP6
EB  OP5  OP4  OP3  OP2  OP1  OP0  VCC

IF (VCC) /OP0 =  /EB*/EA*/IM*/A23*/A22*/A21*/A20*/A19      +
                 /EB*EA*/IM*/A23*/A22*A21*A20*A19          +
                 EB*/EA*/IM*/A23*A22*A21*A20*/A19          +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18   +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*/A17

IF (VCC) /OP1 =  /EB*/EA*/IM*/A23*/A22*/A21*/A20*A19       +
                 /EB*EA*/IM*/A23*A22*/A21*/A20*/A19        +
                 EB*/EA*/IM*/A23*A22*A21*A20*A19           +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A16    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A17    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17*/A16

IF (VCC) /OP2 =  /EB*/EA*/IM*/A23*/A22*/A21*A20*A19        +
                 /EB*EA*/IM*/A23*A22*/A21*/A20*A19         +
                 EB*/EA*/IM*A23*/A22*/A21*/A20*/A19        +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*/A18*A17  +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17

IF (VCC) /OP3 =  /EB*/EA*/IM*/A23*/A22*/A21*A20*A19        +
                 /EB*EA*/IM*/A23*A22*/A21*A20*/A19         +
                 EB*/EA*/IM*A23*/A22*/A21*/A20*A19         +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A17*A16  +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A17 +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18*/A16

IF (VCC) /OP4 =  /EB*/EA*/IM*/A23*/A22*A21*/A20*/A19       +
                 /EB*EA*/IM*/A23*A22*/A21*A20*A19          +
                 EB*/EA*/IM*A23*/A22*/A21*A20*/A19         +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18

IF (VCC) /OP5 =  /EB*/EA*/IM*/A23*/A22*A21*/A20*A19        +
                 /EB*EA*/IM*/A23*A22*A21*/A20*/A19         +
                 EB*/EA*/IM*A23*/A22*/A21*A20*A19          +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A16  +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17  +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A17*/A16 +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*A18

IF (VCC) /OP6 =  /EB*/EA*/IM*/A23*/A22*A21*A20*/A19        +
                 /EB*EA*/IM*/A23*A22*A21*/A20*A19          +
                 EB*/EA*/IM*A23*/A22*A21*/A20*/A19         +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*/A19*A18*A17  +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A18    +
                 EB*EA*/IM*/A23*/A22*/A21*/A20*A19*/A17
```

Table B-3. U158 PAL Programming for iSBC® Ø12CX Board (continued)

DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC 012CX
ACCORDING TO THE FOLLOWING TABLE:

EB	EA	OP#	STARTING ADDRESS	
0	0	0	OK	(000000H)
0	0	1	512K	(080000H)
0	0	2	1024K	(100000H)
0	0	3	1536K	(180000H)
0	0	4	2048K	(200000H)
0	0	5	2560K	(280000H)
0	0	6	3072K	(300000H)
0	1	0	3584K	(380000H)
0	1	1	4096K	(400000H)
0	1	2	4608K	(480000H)
0	1	3	5120K	(500000H)
0	1	4	5632K	(580000H)
0	1	5	6144K	(600000H)
0	1	6	6656K	(680000H)
1	0	0	7168K	(700000H)
1	0	1	7680K	(780000H)
1	0	2	8192K	(800000H)
1	0	3	8704K	(880000H)
1	0	4	9216K	(900000H)
1	0	5	9728K	(980000H)
1	0	6	10240K	(A00000H)
1	1	0	OK W/DESEL	(00H)
1	1	1	64K	(010000H)
1	1	2	128K	(020000H)
1	1	3	192K	(030000H)
1	1	4	256K	(040000H)
1	1	5	320K	(050000H)
1	1	6	384K	(060000H)

```
F F F F F F F F F F F F F F F F F F F F F F F F F F F F .
F 0 F 0 F F F F F F F F F F F F 5 A F F 3 C F F F 0 F 0 F 0 F 0 .
F 0 0 F F F F F F F F F F F F F A 5 F F 6 9 F F E 1 F 0 1 E F 0 .
F 0 F 0 F F F F F F F F F F F F 5 A F F C 3 F F C 3 0 F C 3 3 C .
F 0 0 F 5 F F F 3 F F F F A F F F 0 F F F 0 F F F 0 0 F F 0 F 0 .
F 0 0 F F F F F D E F F 2 F F F F 0 F F F 0 F F F 0 0 F F 0 F 0 .
E 0 0 E E E E E E 2 E E C 2 E E 2 C E E E 0 E E E 0 0 E E 0 E 0 .
A 0 0 A A 0 A A A 8 A A A 0 A A 0 A A A A 0 A A A 0 0 A A 0 A 0 .
B B B B B B B B B B B B B B B B B B B B B B B B B B B B B B .
B 0 B 0 B B B B B B B B B B B B 9 2 B B 3 8 B B 0 B B 0 B 0 B 0 .
B 0 0 B B B B B B B B B B B B B 2 9 B B A 1 B B 1 A B 0 0 B B 0 .
B 0 B 0 B B B B B B B B B B B B 9 2 B B 8 3 B B 3 8 0 B B 0 0 B .
B 0 0 B 9 B B B 3 B B B 0 B B B B 0 B B B 0 B B B 0 0 B B 0 B 0 .
B 0 0 B B B B B 9 B B B 9 2 B B 2 9 B B B 0 B B B 0 0 B B 0 B 0 .
A 0 0 A A 8 A A A 0 A A A A A A 0 A A A A 0 A A A 0 0 A A 0 A 0 .
2 0 0 2 2 2 2 2 2 2 2 2 2 0 2 2 0 2 2 2 2 0 2 2 2 0 0 2 2 0 2 0 .
```

Table B-4. U158 PAL Programming for iSBC® Ø1ØCX Board

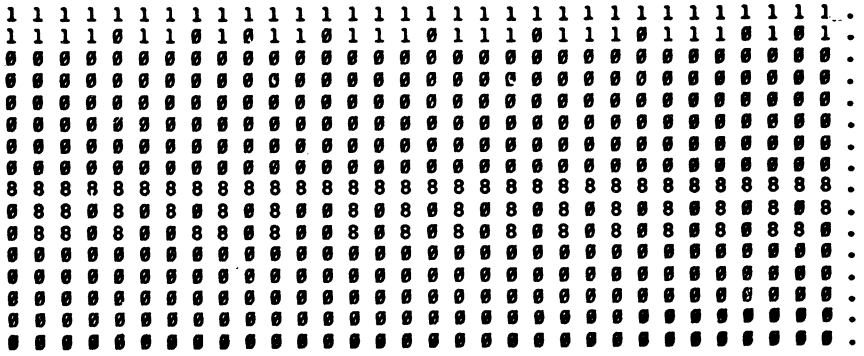
```
PAL16L8A                    PAL DESIGN SPECIFICATION
PXADEC                                        1/27/84
146569 MBCX 1MEG LBX BUS ADDRESS DECODER W/ 3 DESELECTS

EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OP0 VCC

IF (VCC) OP0 = /EB*/EA*/IM*/A23*/A22*/A21*/A20          +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A18      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A17*/A16

IF (VCC) OP1 = /EB*/EA*/IM*/A23*/A22*/A21*A20           +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A18      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A17

IF (VCC) OP2 = /EB*/EA*/IM*/A23*/A22*A21*/A20           +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A18      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A17      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A16

IF (VCC) OP3 = /EB*/EA*/IM*/A23*/A22*A21*A20            +
                EB*EA*/IM*/A23*/A22*/A21*/A20*A19*A18   +
                EB*EA*/IM*/A23*/A22*/A21*A20*/A19       +
                EB*EA*/IM*/A23*/A22*/A21*A20*A19*/A18

IF (VCC) OP4 = /EB*/EA*/IM*/A23*A22*/A21*/A20           +
                EB*EA*/IM*/A23*/A22*/A21*A20

IF (VCC) OP5 = /EB*/EA*/IM*/A23*/A22*A21                +
                EB*EA*/IM*/A23*/A22*/A21*A20*/A19*A18   +
                EB*EA*/IM*/A23*/A22*/A21*A20*A19        +
                EB*EA*/IM*/A23*/A22*A21*/A20*/A19*/A18

IF (VCC) OP6 = /EB*/EA*/IM*A23*A22*/A21                 +
                EB*EA*/IM*/A23*/A22*/A21*A20*A19        +
                EB*EA*/IM*/A23*/A22*A21*/A20*/A19


DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC
 ACCORDING TO THE FOLLOWING TABLE:

EB      EA      OP #          STARTING ADDRESS
Ø       Ø       Ø             ØM      (ØØØØØØH)
Ø       Ø       1             1M      (1ØØØØØH)
Ø       Ø       2             2M      (2ØØØØØH)
Ø       Ø       3             3M      (3ØØØØØH)
Ø       Ø       4             4M      (4ØØØØØH)
Ø       Ø       5             5M      (5ØØØØØH)
Ø       Ø       6             6M      (6ØØØØØH)
1       1       Ø             ØK Deselected 13/16
1       1       1             ØK Deselected 7/8
1       1       2             ØK Deselected 15/16
1       1       3             768K    (ØC ØØØØH)
1       1       4            1Ø24K    (1ØØØØØH)
1       1       5            128ØK    (14ØØØØH)
1       1       6            1536K    (18ØØØØH)
```

Table B-5. U158 PAL Programming for iSBC® Ø2ØCX Board

```
PAL16L8                    PAL DESIGN SPECIFICATION
PXADEC                                        1/27/84
146570 MBCX 2M LBX ADDRESS DECODER W/ 7/8 MEG DESELECT

EA IM A16 A17 A18 A19 A20 A21 A22 GND A23 /OP6
EB /OP5 /OP4 /OP3 /OP2 /OP1 /OPØ VCC

IF (VCC) OPØ = /EB*/EA*/IM*/A23*/A22*/A21              +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A19      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A18      +
                EB*EA*/IM*/A23*/A22*/A21*/A20*/A17

IF (VCC) OP1 = /EB*/EA*/IM*/A23*/A22*A21               +
                EB*EA*/IM*/A23*/A22*/A21*A16            +
                EB*EA*/IM*/A23*/A22*/A21*A17            +
                EB*EA*/IM*/A23*/A22*/A21*A18            +
                EB*EA*/IM*/A23*/A22*/A21*A19            +
                EB*EA*/IM*/A23*/A22*/A21*A20            +
                EB*EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*/A17*/A16

IF (VCC) OP2 = /EB*/EA*/IM*/A23*A22*/A21               +
                EB*EA*/IM*/A23*/A22*/A21*A17            +
                EB*EA*/IM*/A23*/A22*/A21*A18            +
                EB*EA*/IM*/A23*/A22*/A21*A19            +
                EB*EA*/IM*/A23*/A22*/A21*A20            +
                EB*EA*/IM*/A23*/A22*A21*/A20*/A19*/A18*/A17

IF (VCC) OP3 = /EB*/EA*/IM*/A23*A22*A21                +
                EB*EA*/IM*/A23*/A22*/A21*A20            +
                EB*EA*/IM*/A23*/A22*A21*/A20

IF (VCC) OP4 = /EB*/EA*/IM*A23*/A22*/A21               +
                EB*EA*/IM*A23*/A22*/A21

IF (VCC) OP5 = /EB*/EA*/IM*A23*/A22*A21                +
                EB*EA*/IM*A23*/A22*A21

IF (VCC) OP6 = /EB*/EA*/IM*A23*A22*/A21                +
                EB*EA*/IM*A23*A22*/A21

DESCRIPTION:

THIS PROGRAM ASSIGNS STARTING ADDRESS FOR SBC
 ACCORDING TO THE FOLLOWING TABLE:

EB      EA      OP #          STARTING ADDRESS
Ø       Ø       Ø             ØM      (ØØØØØØH)
Ø       Ø       1             2M      (2ØØØØØH)
Ø       Ø       2             4M      (4ØØØØØH)
Ø       Ø       3             6M      (6ØØØØØH)
Ø       Ø       4             8M      (8ØØØØØH)
Ø       Ø       5             1ØM     (AØØØØØH)
Ø       Ø       6             12M     (CØØØØØH)
1       1       Ø             ØK DESELECTED TO
                                 7/8 MEGABYTE
1       1       1             64K     (Ø1ØØØØH)
1       1       2             128K    (Ø2ØØØØH)
1       1       3             1M      (1ØØØØØH)
1       1       4             8M      (8ØØØØØH)
1       1       5             1ØM     (AØØØØØH)
1       1       6             12M     (CØØØØØH)
```

Table B-6. U152 PAL Programming

```
/A8 /AB /A7 /A6 /A5 /A4 /A3 /A2 /A1 GND /A0 /OUT1 /A9
/AA /AC /AD AEAF OP1 /OUT2 VCC

IF (VCC) /OUT1 = /OP1*/A0*/A1*/A2*/A3*/A4*/A5*A6*A7*A8*/A9*/AA*/AB*
                 /AC*/AD*/AEAF                                      +
                 OP1*A0*/A1*/A2*/A3*/A4*/A5*A6*A7*A8*/A9*/AA*/AB*
                 /AC*/AD*/AEAF
IF (VCC) /OUT2 = /OP1*/A0*/A1*/A2*/A3*/A4*/A5*A6*/A7


DESCRIPTION:

THE PROGRAM ASSIGNS AN I/O ADDRESS ACCORDING TO THE FOLLOWING
TABLE:

OP1          OUT1                          OUT2

 0     01C0 41C0 81C0 C1C0 : 01C1 41C1 81C1 C1C1
                           :
 1       40   40   40   40 : USER PROGRAMMABLE
```



INDEX

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